HINDUSTHAN COLLEGE OF ENGINEERING AND TECHNOLOGY

(An Autonomous Institution Affiliated to Anna University, Chennai)

(Approved by AICTE, New Delhi, Accredited by NAAC with 'A' Grade)

Coimbatore - 641 032.

M.E APPLIED ELECTRONICS

HINDUSTHAN EDUCATIONAL AND CHARITABLE TRUST

HICET

Curriculum & Syllabus

2020-2021

VISION AND MISSION OF THE INSTITUTION

VISION

To become a premier institution by producing professionals with strong technical knowledge, innovative research skills and high ethical values.

MISSION

IM1: To provide academic excellence in technical education through novel teaching methods.

IM2: To empower students with creative skills and leadership qualities.

IM3: To produce dedicated professionals with social responsibility.

HINDUSTHAN ACADEMIC COUNCIL * HINDUSTHAN COLLEGE OF ENGG & TECH * Chairman

Chairman - BoS
EEE - HiCET

Dean (Academics)
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HINDUSTHAN COLLEGE OF ENGG & TECH * CBE-32 *

VISION AND MISSION OF THE DEPARTMENT

VISION

To become a Centre of Excellence in Electrical and Electronics Engineering, in every facet of Engineering Education.

MISSION

M1. Provide a solid foundation in basic science, mathematics and engineering fundamentals enhancing the student's capability to identify, formulate, analyze and develop solutions for Engineering problems.

M2. Create an ambiance for the students to develop and flourish their technical skills, design knowledge and innovative ideas to address the environmental issues and sustainable development of the society.

M3. Inculcate moral values and leadership qualities to meet the challenges of life with courage and confidence.

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PROGRAM OUTCOMES (POs)

Engineering Graduates will be able to:

PO 1. **Engineering knowledge**: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.

PO 2. **Problem analysis**: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.

PO 3. **Design/development of solutions**: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.

PO 4. **Conduct investigations of complex problems**: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.

PO 5. **Modern tool usage**: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.

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PO 6. **The engineer and society**: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.

PO 7. **Environment and sustainability**: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.

PO 8. **Ethics**: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.

PO 9. **Individual and team work**: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.

PO10. **Communication:** Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.

PO11. **Project management and finance:** Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.

PO12. **Life-long learning:** Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

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PROGRAM SPECIFIC OUTCOMES (PSOs)

PSO 1. To analyze, design and implement solutions for simple and complex engineering problems that are economically feasible, eco-friendly and socially acceptable solutions in the field of Applied Electronics.

PSO 2. To apply research and project management skills in Applied Electronics domain concerned with communication system by employing recent technologies.

PROGRAM EDUCATIONAL OBJECTIVES (PEOs)

PEO 1. To enable graduates to develop solutions to real world problems in the frontier areas of Applied Electronics.

PEO 2. To enable the graduates to adapt to the latest trends in technology through self-learning and to pursue research to meet out the demands in industries and Academia.

PEO 3. To enable the graduates to exhibit leadership skills and enhance their abilities through lifelong learning.

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CURRICULUM

DETAILS OF CHANGES CARRIED OUT IN CURRICULUM & SYLLABUS

CBCS PATTERN

POSTGRADUATE PROGRAMMES

M.E APPLIED ELECTRONICS – R2020

For the students admitted during the academic year 2020-2021 and onwards

SEMESTER I

S.No.	Course Code	Course Title	Category	L	T	P	C	CIA	ESE	TOTAL
THEORY										
1	20MA1102	Advanced Mathematics for Electrical and Electronics Engineering	BS	3	0	0	3	40	60	100
2	20AE1201	Advanced Digital System Design	PC	3	0	0	3	40	60	100
3	20AE1202	Embedded System Design	PC	3	0	0	3	40	60	100
4	20AE1203	Digital Image Processing	PC	3	0	0	3	40	60	100
5	20AE1204	Research Methodology	PC	3	0	0	3	40	60	100
PRACTICAL										
6	20AE1001	Electronic System Design Laboratory	PC	0	0	4	2	50	50	100
7	20AE1002	Embedded System Laboratory	PC	0	0	4	2	50	50	100
MANDATORY COURSE										
8	20AC10XX	AUDIT COURSE I	AC	2	0	0	0	100	0	100
Total Credits:				**17**	**0**	**8**	**19**	**400**	**400**	**800**

SEMESTER II

S.No.	Course Code	Course Title	Category	L	T	P	C	CIA	ESE	TOTAL
THEORY										
1	20AE2201	Analog Integrated Circuit Design	PC	3	0	0	3	40	60	100
2	20AE2202	VLSI Design Techniques	PC	3	0	0	3	40	60	100
3	20AE23XX	**Professional Elective I**	PE	3	0	0	3	40	60	100
4	20AE23XX	**Professional Elective II**	PE	3	0	0	3	40	60	100
5	20AE23XX	**Professional Elective III**	PE	3	0	0	3	40	60	100
PRACTICAL										
6	20AE2001	VLSI Design Laboratory	PC	0	0	4	2	50	50	100
7	20AE2901	MINI PROJECT	PC	2	0	0	2	50	50	100
MANDATORY COURSE										
8	20AC20XX	AUDIT COURSE II	AC	2	0	0	0	100	0	100
Total Credits:				**19**	**0**	**4**	**19**	**400**	**400**	**800**

LIST OF PROFESSIONAL ELECTIVES

PROFESSIONAL ELECTIVE I

S.No.	Course Code	Course Title	Category	L	T	P	C	CIA	ESE	TOTAL
THEORY										
1	20AE2301	Advanced Digital Signal Processing	PE	3	0	0	3	40	60	100
2	20AE2302	Advanced Microprocessors and Microcontrollers	PE	3	0	0	3	40	60	100
3	20AE2303	ASIC and FPGA Design	PE	3	0	0	3	40	60	100

PROFESSIONAL ELECTIVE II

S.No.	Course Code	Course Title	Category	L	T	P	C	CIA	ESE	TOTAL
THEORY										
1	20AE2304	Computer Architecture and Parallel Processing	PE	3	0	0	3	40	60	100
2	20AE2305	CAD for VLSI Design	PE	3	0	0	3	40	60	100

PROFESSIONAL ELECTIVE III

S.No.	Course Code	Course Title	Category	L	T	P	C	CIA	ESE	TOTAL
THEORY										
1	20AE2307	Electromagnetic Interference and Compatibility	PE	3	0	0	3	40	60	100
2	20AE2308	Wireless Adhoc and Sensor Networks	PE	3	0	0	3	40	60	100
3	20AE2309	Robotics and Intelligent Systems	PE	3	0	0	3	40	60	100

For the students admitted during the academic year 2019-2020 and onwards

SEMESTER III

S.No.	Course Code	Course Title	L	T	P	C	CIA	ESE	TOTAL
THEORY									
1	16AP3201	Computer Architecture and Parallel Processing	3	0	0	3	40	60	100
2	16AP33XX	**Professional Elective V**	3	0	0	3	40	60	100
3	16AP33XX	**Professional Elective VI**	3	0	0	3	40	60	100
PRACTICAL									
4	16AP3001	Electronics System Design Laboratory	0	0	4	2	50	50	100
5	16AP3901	Project Phase – I	0	0	12	6	50	50	100
Total Credits:			**9**	**0**	**16**	**17**	**220**	**280**	**500**

SEMESTER IV

S.No.	Course Code	Course Title	L	T	P	C	CIA	ESE	TOTAL
PRACTICAL									
1	16AP4902	Project Phase - II	0	0	24	12	100	100	200
Total Credits:			**0**	**0**	**24**	**12**	**100**	**100**	**200**

LIST OF PROFESSIONAL ELECTIVES

PROFESSIONAL ELECTIVE V

S.No.	Course Code	Course Title	L	T	P	C	CIA	ESE	TOTAL
THEORY									
1	16AP3301	Testing of VLSI Circuits	3	0	0	3	40	60	100
2	16AP3302	Photonics	3	0	0	3	40	60	100
3	16AP3303	Nano Electronics	3	0	0	3	40	60	100
4	16AP3304	Internetworking and Multimedia	3	0	0	3	40	60	100
5	16AP3305	ASIC Design	3	0	0	3	40	60	100

PROFESSIONAL ELECTIVE VI

S.No.	Course Code	Course Title	L	T	P	C	CIA	ESE	TOTAL
THEORY									
1	16AP3306	Robotics	3	0	0	3	40	60	100
2	16AP3307	MEMS and NEMS	3	0	0	3	40	60	100
3	16AP3308	System on Chip Design	3	0	0	3	40	60	100
4	16AP3309	Wireless Adhoc and Sensor Networks	3	0	0	3	40	60	100
5	16AP3310	Applied Medical Image Processing	3	0	0	3	40	60	100

CREDIT DISTRIBUTION (R2020)

Semester	I	II	III	IV	TOTAL
Credits	19	19	19	15	72

CREDIT DISTRIBUTION (R2016)

Semester	I	II	III	IV	TOTAL
Credits	23	23	17	12	75

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SYLLABUS

SEMESTER-I

PROGRAMME	COURSE CODE	NAME OF THE COURSE	L	T	P	C
M.E.	20MA1102	ADVANCED MATHEMATICS FOR ELECTRICAL AND ELECTRONICS ENGINEERING	3	0	0	3

Course Objective

1. Apply testing of hypothesis to infer outcome of experiments.
2. Formulate and construct a mathematical model for a linear programming problem in real life situation.
3. Understand the network modeling for planning and scheduling the project activities.
4. Develop the ability to use the concepts of Linear Algebra and Special functions for
5. Acquire knowledge of Fuzzy logic and Fuzzy Algebra.

Unit	Description	Instructional Hours
I	**TESTING OF HYPOTHESES** Sampling distributions -Type I and Type II errors - Tests based on Normal, t, Chi-Square and F distributions for testing of mean, variance and proportions -Tests for Independence of attributes and Goodness of fit.	9
II	**LINEAR PROGRAMMING** Formulation - Graphical solution - Simplex method - Artificial variable Techniques - Transportation and Assignment Models	9
III	**SCHEDULING BY PERT AND CPM** Network Construction - Critical Path Method - Project Evaluation and Review technique - Resource Analysis in Network Scheduling.	9
IV	**LINEAR ALGEBRA** Vector spaces – norms - Inner Products - Eigen values using QR Factorization - generalized eigenvectors - Canonical forms - singular value decomposition and applications -pseudo inverse - least square approximations -Toeplitz matrices and some applications.	9
V	**FUZZY LOGIC AND FUZZY ALGEBRA** Basic principles of Fuzzy logic - Fuzzy sets of operations - Fuzzy membership Matrix.	9
	Total Instructional Hours	**45**

Course Outcome

CO1: Acquire the basic concepts of Probability and Statistical techniques for solving mathematical problem which will be useful in solving engineering problems.
CO2: Apply transportation and assignment models to find optimal solution in warehousing and travelling.
CO3: Prepare project scheduling using PERT and CPM.
CO4: Achieve an understanding of the basic concepts of algebraic equations and method of solving
CO5: Apply the Fuzzy logic in power system problems.

TEXT BOOK

T1 -Richard Bronson, Gabriel B.Costa, "Linear Algebra", Academic Press, Second Edition,2007.
T2 -Richard Johnson, "Miller & Freund's Probability and Statistics for Engineer", Prentice –Hall, 7th Edition, 2007.
T3 - Taha H.A,"Operations Research, An Introduction "8th Edition, Pearson Education, 2008.

REFERENCE BOOKS

R1 -Gupta S.C. and Kapoor V.K."Fundementals of Mathematical Statistics", Sultan an Sons,2001.
R2 -Prem Kumar Gupta,D.S.Hira,"Operations Research," S.Chand &Company Ltd, New Delhi,3rd edition,2008.
R3- Panner Selvam,Operations Research",Prentice Hall of India,2002.
R4- George J.Klir and Yuan,B., Fuzzy sets and fuzzy logic, Theory and applications, Prentice Hall of India Pvt.Ltd., 1997.

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PROGRAMME	COURSE CODE	NAME OF THE COURSE	L	T	P	C
M.E.	20AE1201	ADVANCED DIGITAL SYSTEM DESIGN	3	0	0	3

Course Objective

1. Basic concepts of Sequential Circuit Design.
2. Basic concepts of Asynchronous Sequential Circuit Design.
3. Learn the concepts of fault modeling and fault - tolerant systems
4. Study the concepts of programmable logic devices.
5. Apply the concepts of System Design Using Verilog and Programmable Devices

Unit	Description	Instructional Hours
I	**SEQUENTIAL CIRCUIT DESIGN** Analysis of clocked synchronous sequential circuits and modeling- State diagram, state table, state table assignment and reduction-Design of synchronous sequential circuits - ASM chart and realization using ASM.	9
II	**ASYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN** Analysis of asynchronous sequential circuit – flow table reduction-races-state assignment-transition table and problems in transition table- design of asynchronous sequential circuit-Static, dynamic and essential hazards – data synchronizers – mixed operating mode asynchronous circuits – designing vending machine controller	9
III	**FAULT DIAGNOSIS AND TESTABILITY ALGORITHMS** Fault table method-path sensitization method – Boolean difference method-D algorithm - Tolerance techniques – The compact algorithm – Fault in PLA – Test generation-DFT schemes – Built in self-test.	9
IV	**SYNCHRONOUS DESIGN USING PROGRAMMABLE DEVICES** Programming logic device families – Designing a synchronous sequential circuit using PLA/PAL – Realization of finite state machine using PLD – FPGA – Xilinx FPGA-Xilinx 4000	9
V	**SYSTEM DESIGN USING VERILOG** Hardware Modelling with Verilog HDL – Logic System, Data Types and Operators For Modelling in Verilog HDL - Behavioral Descriptions in Verilog HDL – HDL Based Synthesis – Synthesis of Finite State Machines– structural modeling – compilation and simulation of Verilog code –Test bench - Realization of combinational and sequential circuits using Verilog – Registers – counters – sequential machine – serial adder – Multiplier- Divider – Design of simple microprocessor.	9
	Total Instructional Hours	**45**

Course Outcome

CO1: Design and analysis of sequential circuit.
CO2: Design and analysis of asynchronous sequential circuit.
CO3: Explore fault diagnosis and testability algorithm
CO4: Learn of programmable logic devices.
CO5: Design and analysis of hardware description languages.

TEXT BOOKS:

T1 Charles H.Roth Jr "Fundamentals of Logic Design" Thomson Learning 2004

T2 M.D.Ciletti , Modeling, Synthesis and Rapid Prototyping with the Verilog HDL, Prentice Hall, 1999.

REFERENCE BOOKS:

R1 M.G.Arnold, Verilog Digital – Computer Design, Prentice Hall (PTR), 1999.

R2 Parag K.Lala "Digital system Design using PLD" B S Publications,2003

R3 Nripendra N Biswas "Logic Design Theory" Prentice Hall of India,2001

R4 Parag K.Lala "Fault Tolerant and Fault Testable Hardware Design" B S Publications,2002

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PROGRAMME	COURSE CODE	NAME OF THE COURSE	L	T	P	C
M.E.	20AE1202	EMBEDDED SYSTEM DESIGN	3	0	0	3

Course Objective

1. Understand the design challenges and methodologies of embedded system
2. Study general and single purpose processor and its developement
3. Understand bus structures
4. Learn the embedded system design procedurs for various processes
5. Study the embedded software tools for RTOS

Unit	Description	Instructional Hours
I	**EMBEDDED SYSTEM OVERVIEW** Embedded System Overview, Design Challenges – Optimizing Design Metrics, Design Methodology, RT-Level Combinational and Sequential Components, Optimizing Custom Single-Purpose Processors.	9
II	**GENERAL AND SINGLE PURPOSE PROCESSOR** Basic Architecture, Pipelining, Superscalar and VLIW architectures, Development Environment: Application-Specific Instruction-Set Processors (ASIPs) Microcontrollers, Timers, Counters and watchdog Timer, UART and Analog-to-Digital Converters, Memory Concepts.	9
III	**BUS STRUCTURES** Basic Protocol Concepts, Microprocessor Interfacing – I/O Addressing, Port and Bus-Based I/O, Arbitration, Serial Protocols, I^2C, CAN and USB, Parallel Protocols – PCI and ARM Bus, Wireless Protocols – IRDA, Bluetooth, IEEE 802.11.	9
IV	**STATE MACHINE AND CONCURRENT PROCESS MODELS** Basic State Machine Model, Finite-State Machine with Data path Model, Concurrent Process Model, Communication among Processes, Synchronization among processes, Dataflow Model, Real-time Systems, Automation: Synthesis, Intellectual Property Cores, Design Process Models.	9
V	**EMBEDDED SOFTWARE DEVELOPMENT TOOLS AND RTOS** Compilation Process – Libraries – Porting kernels – C extensions for embedded systems – Emulation and debugging techniques – RTOS – System design using RTOS.	9
	Total Instructional Hours	**45**

Course Outcome

CO1: Identify the various embedded system design
CO2: Evaluate the general and single purpose processors
CO3: Compare various bus structures
CO4: Recognize the process models
CO5: Apply the embedded software development tools

TEXT BOOKS:

T1 Bruce Powel Douglas, "Real time UML, second edition: Developing efficient objects for embedded systems", 3rd Edition 1999, Pearson Education.

T2 Frank Vahid and Tony Gwargie, "Embedded System Design", John Wiley & sons, 2002.

REFERENCE BOOKS:

R1 Daniel W.Lewis, "Fundamentals of embedded software where C and assembly meet", Pearson Education, 2002.

R2 Steve Heath, "Embedded System Design", Elsevier, Second Edition, 2004.

R3 Jonathan W.Valvano: "Embedded Microcomputer Systems – Real Time Interfacing", Cengage Learning; Third of later edition

R4 Osborn.G, "Embedded microcontroller and p0rocessor design", Pearson

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PROGRAMME	COURSE CODE	NAME OF THE COURSE	L	T	P	C
M.E.	20AE1203	DIGITAL IMAGE PROCESSING	3	0	0	3

COURSE OBJECTIVE

1. To understand the fundamentals of Digital Image
2. To analyze and design the Image transforms and Enhancement.
3. To study and analyze the operation of Image restoration and construction.
4. To study and understand the Image compression & Segmentation.
5. To understand color and multispectral image processing.

Unit	Description	Instructional Hours
I	**Digital Image Fundamentals.** Introduction: Digital Image- Steps of Digital Image Processing Systems-Elements of Visual Perception -Connectivity and Relations between Pixels. Simple Operations- Arithmetic, Logical, Geometric Operations. Mathematical Preliminaries - 2D Linear Space Invariant Systems - 2D Convolution - Correlation 2D Random Sequence - 2D Spectrum.	9
II	**Image Transforms and Enhancement.** Image Transforms: 2D Orthogonal and Unitary Transforms-Properties and Examples. 2D DFT-FFT – DCT -Hadamard Transform - Haar Transform - Slant Transform - KL Transform - Properties And Examples.Image Enhancement:- Histogram Equalization Technique- Point Processing-Spatial Filtering-In Space And Frequency - Nonlinear Filtering-Use Of Different Masks.	9
III	**Image restoration and construction.** Image Restoration: Image Observation And Degradation Model, Circulant And Block Circulant Matrices and Its Application In Degradation Model - Algebraic Approach to Restoration-Inverse By Wiener Filtering – Generalized Inverse-SVD and Interactive Methods - Blind Deconvolution-Image Reconstruction From Projections.	9
IV	**Image compression & segmentation** Image Compression: Redundancy And Compression Models -Loss Less And Lossy. Loss Less-Variable-Length, Huffman, Arithmetic Coding - Bit-Plane Coding, Loss Less Predictive Coding, LossyTransform (DCT) Based Coding, JPEG Standard - Sub Band Coding. Image Segmentation: Edge Detection - Line Detection - Curve Detection - Edge Linking And Boundary Extraction, Boundary Representation, Region Representation And Segmentation, Morphology-Dilation, Erosion, Opening And Closing. Hit And Miss Algorithms Feature Analysis	9
V	**Color and multispectral image processing** Color Image-Processing Fundamentals, RGB Models, HSI Models, Relationship Between Different Models. Multispectral Image Analysis - Color Image Processing Three Dimensional Image Processing-Computerized Axial Tomography-Stereometry-Stereoscopic Image Display-Shaded Surface Display.	9
	TOTAL INSTRUCTIONAL HOURS	**45**

COURSE OUTCOME

At the end of this course, students will be able to
CO1: Identify various arithmetic and geometrical operations of image fundamental.
CO2: Analyze the operation Image transforms and Enhancement.
CO3: Design Image compression and restoration techniques.
CO4: Design the Image compression and Segmentation.
CO5: Create models for color and multispectral image processing.

TEXT BOOKS:

T1 Digital Image Processing, Gonzalez.R.C & Woods. R.E., 3/e, Pearson Education, 2008.
T2 Digital Image Processing, Kenneth R Castleman, Pearson Education,1995.

REFERENCES:

R1 1. Digital Image Procesing, S. Jayaraman, S. Esakkirajan, T. Veerakumar, McGraw Hill Education ,2009
R2 2.Fundamentals of Digital image Processing, Anil Jain.K, Prentice Hall of India, 1989.
R3 3.Image Processing, Sid Ahmed, McGraw Hill, New York, 1995
R4 4.Image Processing: The Fundamentals, Maria Petrou,Costas Petrou,Wiley,2010

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PROGRAMME	COURSE CODE	NAME OF THE COURSE	L	T	P	C
M.E.	20AE1204	RESEARCH METHODOLOGY	3	0	0	3

Course Objectives

1. Impart scientific knowledge for carrying out research work effectively.
2. Understand the concepts in various research designs.
3. Acquire knowledge about Experimental design and Data collection
4. Confer about the multivariate analysis techniques
5. Disseminate knowledge on Research Practices and Report writing.

Unit	Description	Instructional hours
I	**INTRODUCTION TO RESEARCH** Research-Definition-Objectives of research, Meaning of research- Characteristics of research -Importance of research activities- Types of research-Research approaches-Significance-Problems in research-Qualities of good researcher- Research process.	9
II	**RESEARCH DESIGN** Formulation of the research design: Process-classification of research designs-Exploratory-Secondary resource analysis-Two-tired research design- -Validity in experimentation-factors affecting external validity-classification of experimental design - Pre-experimental- Quasi-experimental designs.	9
III	**DATA COLLECTION METHODS** Classification of Data-Collection of primary data-Observation-Interview method-Collection of data through Questionnaires-schedules-collection of secondary data-Research applications of secondary data-Benefits and drawbacks-classification of secondary data-Internal –External data sources.	9
IV	**MULTIVARIATE ANALYSIS TECHNIQUES** Growth of Multivariate techniques-Characteristics and applications-Classification-Variables in multivariate analysis-Important multivariate techniques-Factor analysis-Rotation in factor analysis-R-type and Q type factor analysis-Path analysis.	9
V	**RESEARCH PRACTICE AND REPORT WRITING.** Literature review-Conference Proceedings-Journals-Journal Impact Factor (JFI)-Citation index-h-index-Significance of report writing-Different steps in writing report-Layout of report writing-Types of reports-Mechanics of writing a research report-precautions for writing research reports-Conclusion and Scope for future work-Oral presentation.	9
	Total instructional hours	**45**

Course Outcomes

CO1: Observe the various approaches to do research.
CO2: Carryout the research design.
CO3: Evaluate the data collection for research activities.
CO4: Acknowledge the function of Multivariate Analysis Techniques
CO5: Organize the research activity systematically and prepare research report effectively.

TEXT BOOKS:

T1. C.R. Kothari, Research Methodology Methods &Techniques, NEW Age International (P) Limited, New Delhi, 2007.

T2. Dr. Deepak Chawla, Dr. Neena Sondhi, Research Methodology concepts and cases, Vikas Publishing House Pvt. Ltd., New Delhi, 2011

REFERENCE BOOKS:

R1. K. Prathapan, Research Methodology for Scientific Research, I.K. International Publishing House Pvt. Ltd. New Delhi, 2014L.

R2. R. Panneerselvam, Research Methodology, PHI Learning Private Limited, New Delhi, 2011.

R3. Donald H. McBurney, Research Methods, Thomson Asia Pvt. Ltd. Singapore, 2002.

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PROGRAMME	COURSE CODE	NAME OF THE COURSE	L	T	P	C
M.E.	20AE1001	ELECTRONIC SYSTEM DESIGN LABORATORY	0	0	4	2

Course Objective

1. Impart the knowledge on Interfacing of different Processor.
2. Testing of flash controller programming.
3. Analyze of process control and PCB designing.
4. Intend and analysis of modulator and demodulator.
5. Design system using instrumentation amplifier.

Expt. No.	Description of the experiments
1	Study of different interfaces (using Embedded Microcontroller).
2	Flash Controller Programming Data flash, with erase, verify and Fusing.
3	Design of Wireless Data Modem.
4	PCB layout design using CAD tool.
5	Design of Process Control Timer.
6	Design of AC/DC voltage regulator using SCR.
7	Design of an Instrumentation Amplifier.
8	Implementation of Adaptive filters and multistage multi-rate system in DSP processor.
9	Sensor design using simulation tools.
10	Design of Temperature sensor using Instrumentation Amplifier.

Total Practical Hours 45

Course Outcome

CO1: Design various analog / digital transceiver systems and control different process.
CO2: Analyze flash controller programming and wireless data modem.
CO3: Analyze PCB designing for various circuits.
CO4: Propose interfaces using modulator and demodulator.
CO5: Design and analysis of operational and instrumentation amplifiers.

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PROGRAMME	COURSE CODE	NAME OF THE COURSE	L	T	P	C
M.E.	20AE1002	EMBEDDED SYSTEMS LABORATORY	0	0	4	2

Course Objective

1. Impart the knowledge on various analog / digital transceiver systems and control different process.
2. Design system using 8086 and 8051 Microcontroller.
3. Study and design wireless network using embedded systems.
4. Study the different interfaces using Embedded Microcontroller.
5. Intend and analysis of real time operating system.

Expt. No.	Description of the experiments
1	System design using PIC Micro controller and its applications.
2	Testing of RTOS environment and system programming using ARM7 Processor.
3	System design using 8051 Micro Controller, 8086 Micro Processor.
4	RTC using PIC Micro Controller.
5	Elevator controller using PIC Micro Controller.
6	Modern Train Controller using PIC micro controller.
7	Study of MSP430 and 8086-16 bit Microprocessor its applications
8	Designing of Wireless Network using Embedded System.
9	Sensor design using simulation tools.
10	Study of 32 bit ARM7 microcontroller RTOS and its applications

Total Practical Hours 45

Course Outcome

CO1: Design various analog / digital transceiver systems and control different process.
CO2: Propose interfaces using embedded Microcontroller.
CO3: Experiment Wireless Network Using Embedded Systems.
CO4: Analyze the system using 8086 and 8051 Microcontroller.
CO5: Design and Analysis of Real Time Operating System

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SEMESTER-II

PROGRAMME	COURSE CODE	NAME OF THE COURSE	L	T	P	C
M.E.	20AE2201	ANALOG INTEGRATED CIRCUIT DESIGN	3	0	0	3

Course Objectives

1. Design the single stage amplifiers using pmos and nmos driver circuits with different loads.
2. Analyze high frequency concepts of single stage amplifiers and noise characteristics associated with differential amplifiers.
3. Study the different types of current mirrors and to know the concepts of voltage and current reference circuits.
4. Gain the various applications in operational amplifier.
5. Learn the different concepts in stability and frequency compensation

Unit	Description	Instructional hours
I	**SINGLE STAGE AMPLIFIERS** Basic MOS physics and equivalent circuits and models, CS, CG and Source Follower differential with active load, Cascode and folded cascode configurations with active load, Design of differential and cascode amplifiers – to meet specified SR, noise, gain, BW, ICMR and power dissipation, voltage swing, High gain amplifier, structures.	9
II	**HIGH FREQUENCY AND NOISE OF CHARACTERISTICS AMPLIFIERS** Miller effect, association of poles with nodes, frequency response of CS, CG and source follower, cascode and differential pair stages, Statistical characteristics of noise, noise in single stage amplifiers, noise in differential amplifiers.	9
III	**FEEDBACK AND ONE STAGE OPERATIONAL AMPLIFIERS** Properties and types of negative feedback circuits, effect of loading in feedback networks, operational amplifier performance parameters, One-stage Op Amps, Two-stage Op Amps, Input range limitations, Gain boosting, slew rate, power supply rejection, noise in Op Amps.	9
IV	**STABILITY AND FREQUENCY COMPENSATION OF TWO STAGE AMPLIFIER** Analysis of two stage Op amp – two stage Op amp single stage CMOS Cs as second stage and using cascode second stage, multiple systems, Phase Margin, Frequency Compensation, and Compensation of two stage Op Amps, Slewing in two stage Op Amps, Other compensation techniques.	9
V	**BANDGAP REFERENCES** Current sinks and sources, Current mirrors, Wilson current source, Wildar current source, Cascode current source, Design of high swing cascode sink, current amplifiers, Supply independent biasing, temperature independent references, PTAT and CTAT current generation, Constant-Gm Biasing.	9
	Total instructional hours	**45**

Course Outcomes

CO1: Design and analysis of amplifiers.
CO2: Aquire of frequency response and noise analysis.
CO3: Familiarize the Operational Amplifiers.
CO4: Compose different types of Biasing Circuits.
CO5: Gain knowledge about the engineering applications of Analog Integrated Circuits

TEXT BOOKS:

T1. Behzad Razavi, "Design of Analog CMOS Integrated Circuits", Tata McGraw Hill, 2001
T2. Willey M.C. Sansen, "Analog Design Essentials", Springer, 2006.

REFERENCE BOOKS:

R1. Grebene, "Bipolar and MOS Analog Integrated Circuit Design", John Wiley & sons,Inc.,2003.
R2. Phillip E.Allen, Douglas R.Holberg, "CMOS Analog Circuit Design", Oxford University Press, 2nd Edition, 2002.
R3. Jacob Baker "CMOS: Circuit Design, Layout, and Simulation", Wiley IEEE Press, 3rd Edition, 2010..

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PROGRAMME	COURSE CODE	NAME OF THE COURSE	L	T	P	C
M.E.	20AE2202	VLSI DESIGN TECHNIQUES	3	0	0	3

COURSE OBJECTIVE

To impart knowledge on

1. To understand the fundamentals of MOS transistor theory.
2. To analyze and design the CMOS technologies.
3. To study and discuss characteristics and performance estimation.
4. To study and understand the VLSI system components.
5. To understand Verilog programming.

Unit	Description	Instructional Hours
I	**INTRODUCTION TO MOS TRANSISTOR THEORY** MOS transistors, CMOS logic, MOS transistor theory–Introduction, Enhancement mode transistor action, Ideal I-V characteristics, Simple MOS capacitance Models, Detailed MOS gate capacitance model, Detailed MOS Diffusion capacitance model,Non ideal I-V effects, DC transfer characteristics, VLSI Design flow	9
II	**CMOS TECHNOLOGY AND DESIGN RULE** CMOS fabrication and Layout, CMOS technologies, P-Well process, N-Well process, twin-tub process, MOSlayers stick diagrams and Layout diagram, Layout design rules, Latch up in CMOS circuits, CMOS process enhancements, Technology–related CAD issues, Fabrication and packaging.	9
III	**CIRCUIT CHARACTERISATION & PERFORMANCE ESTIMATION** Determination of Pull-up to Pull-down ratio for NMOS inverter, super buffers, Driving large capacitance loads,Circuits families, transmission gates, Delay estimation, Power dissipation, Design margin, Scaling of MOSCircuits.	9
IV	**VLSI SYSTEM COMPONENTS CIRCUITS** Multiplexers, Decoders, comparators, priority encoders, Shift registers. Arithmetic circuits–Ripple carryadders, Carry look ahead adders, High-speed adders, Multiplier	9
V	**VERILOG HARDWARE DESCRIPTION LANGUAGE** Overview of digital design with Verilog HDL, hierarchical modeling concepts, basic concepts, modules and port definitions, gate level modeling, data flow modeling, behavioral modeling, task & functions, Test Bench.	9
	TOTAL INSTRUCTIONAL HOURS	**45**

COURSE OUTCOME

CO1: Identify various MOS transistor theory
CO2: Analyze the CMOS technology and to design.
CO3: Design and analyze circuit characteristics and Performance.
CO4: Design the VLSI system components and circuits.
CO5: Create models using Verilog programming.

TEXT BOOKS:

T1 Neil H.E.Weste, David Harris and Ayan Banerjee, "CMOS VLSI Design a circuits and systems perspective, Third Edition, Pearson Education, 2010

T2 Douglas A.Pucknell and Kamran Eshraghian, "Basic VLSI Design", Third Edition, Prentice-Hall of India 2004.

REFERENCES:

R1 Samir Palnitkar, "Verilog HDL a Guide to Digital Design and Synthesis", Second Edition, Pearson Education, 2010.

R2 John P.Uyemura "Introductionto VLSI Circuits and Systems", Wiley India Edition, 2006.

R3 Neil H.E. Weste and Kamran Eshraghian, Principles of CMOS VLSI Design, Pearson Education ASIA, 2nd edition, 2000.

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PROGRAMME	COURSE CODE	NAME OF THE COURSE	L	T	P	C
M.E.	20AE2001	VLSI DESIGN LABORATORY	0	0	4	2

Course Objective

1. Learn new software tools for VLSI.
2. Study various design methods for VLSI circuits.
3. Gain the knowledge about circuit designing.
4. Analyze various applicationsusing VHDL and Verilog.
5. Analysis the digital system and simulator.

EXPT. No	Description of the Experiments
1.	Design and Simulation of Arithmetic /logic operator circuits using verilog/VHDL
2.	Design and 8-bit signed multiplication algorithm using verilog / VHDL
3.	Modeling of Combinational/Sequential Circuits Using Verilog HDL
4.	Simulation of Digital Circuits using Xilinx ISE.
5.	Design and Simulation of Digital Circuits using VHDL and Porting them into FPGA.
6.	Layout of Simple NMOS/CMOS Circuits.
7.	Analysis of Asynchronous and clocked synchronous sequential circuits.
8.	Design and Implementation of ALU in FPGA using VHDL and Verilog.
9.	Modeling of Sequential Digital system using Verilog and VHDL.
10.	Modeling of MAC unit using verilog / VHDL

Total Practical Hours 45

Course Outcome

CO1: Use the software tools for designing and simulation.
CO2: Design the various VLSI circuits using VHDL programming.
CO3: Familiarize the applications of VLSI circuits.
CO4: Analysis the MAC unit using verilog.
CO5: Design the VLSI circuits using Xillinx ISE tool.

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PROGRAMME	COURSE CODE	PROFESSIONAL ELECTIVE-I NAME OF THE COURSE	L	T	P	C
M.E.	20AE2301	ADVANCED DIGITAL SIGNAL PROCESSING	3	0	0	3

COURSE OBJECTIVE

To impart knowledge on

1. To understand Discrete-time signal transforms, digital filter design, optimal filtering
2. To analyze and design Power spectrum estimation.
3. To study and analyze the multi-rate digital signal processing
4. To study and Design adaptive Filters.
5. To understand and design multi-rate digital signal processing.

Unit	Description	Instructional Hours
I	**DISCRETE RANDOM SIGNAL PROCESSING** Weiner Khitchine relation - Power spectral density – filtering random process, Spectral Factorization Theorem, special types of random process – Signal modeling-Least Squaresmethod, Pade approximation, Prony's method, iterative Prefiltering, Finite Data records, Stochastic Models	9
II	**SPECTRUM ESTIMATION** Non-Parametric methods - Correlation method - Co-variance estimator - Performance analysisof estimators – Unbiased consistent estimators - Periodogram estimator - Barlett spectrumestimation - Welch estimation - Model based approach - AR, MA, ARMA Signal modeling -Parameter estimation using Yule-Walker method.	9
III	**LINEAR ESTIMATION AND PREDICTION** Maximum likelihood criterion - Efficiency of estimator - Least mean squared error criterion - Wiener filter - Discrete Wiener Hoff equations - Recursive estimators - Kalman filter - Linearprediction, Prediction error - Whitening filter, Inverse filter - Levinson recursion, Lattice realization, Levinson recursion algorithm for solving Toeplitz system of equations.	9
IV	**ADAPTIVE FILTERS** FIR Adaptive filters - Newton's steepest descent method - Adaptive filters based on steepest descent method - Widrow Hoff LMS Adaptive algorithm - Adaptive channel equalization - Adaptive echo canceller - Adaptive noise cancellation - RLS Adaptive filters – Exponentially weighted RLS - Sliding window RLS - Simplified IIR LMS Adaptive filter	9
V	**MULTIRATE DIGITAL SIGNAL PROCESSING** Mathematical description of change of sampling rate - Interpolation and Decimation -Continuous time model - Direct digital domain approach - Decimation by integer factor -Interpolation by an integer factor - Single and multistage realization - Poly phase realization -Applications to sub band coding - Wavelet transform and filter bank implementation of wavelet expansion of signals.	9
	TOTAL INSTRUCTIONAL HOURS	**45**

COURSE OUTCOME

CO1: Identify various arithmetic and geometrical operations for random signals.
CO2: Analyze the spectrum estimation.
CO3: Analyze linear estimation and Prediction.
CO4: Design the adaptive Filters.
CO5: Analyze the multirate digital signal processing.

TEXT BOOKS:

T1 Monson H. Hayes, "Statistical Digital Signal Processing and Modeling", John Wiley and Sons Inc., New York, 2006

T2 Sophoncles J. Orfanidis, "Optimum Signal Processing ", McGraw-Hill, 2000

REFERENCES:

R1 John G. Proakis, Dimitris G. Manolakis, "Digital Signal Processing", Prentice Hall of India, New Delhi, 2005.

R2 Simon Haykin, "Adaptive Filter Theory", Prentice Hall, Englehood Cliffs, NJ1986.

R3 P. P. Vaidyanathan, "Multirate Systems and Filter Banks", Prentice Hall, 1992

R4 N. J. Fliege ,"Multirate Digital Signal Processing: Multirate Systems - Filter Banks – Wavelets", Wiely, 1999.

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PROGRAMME	COURSE CODE	NAME OF THE COURSE	L	T	P	C
M.E.	20AE2302	ADVANCED MICROPROCESSORS & MICROCONTROLLERS	3	0	0	3

Course Objective

1. To expose the students to the fundamentals of microprocessor architecture.
2. To explore the high performance features in CISC architecture
3. To familiarize the high performance features in RISC architecture
4. To introduce the basic features in Motorola microcontrollers.
5. To enable the students to understand PIC Microcontroller

Unit	Description	Instructional Hours
I	**MICROPROCESSOR ARCHITECTURE** Instruction Set – Data formats –Addressing modes – Memory hierarchy –register file – Cache – Virtual memory and paging – Segmentation- pipelining –the instruction pipeline – pipeline hazards – instruction level parallelism – reduced instruction set –Computer principles – RISC versus CISC.	9
II	**HIGH PERFORMANCE CISC ARCHITECTURE – PENTIUM** CPU Architecture- Bus Operations – Pipelining – Brach predication – floating point unit- Operating Modes – Paging – Multitasking – Exception and Interrupts – Instruction set – addressing modes – Programming the Pentium processor.	9
III	**HIGH PERFORMANCE RISC ARCHITECTURE – ARM** Organization of CPU – Bus architecture –Memory management unit - ARM instruction set- Thumb Instruction set- addressing modes – Programming the ARM processor.	9
IV	**MSP430 16 - BIT MICROCONTROLLER** The MSP430 Architecture- CPU Registers - Instruction Set, On-Chip Peripherals - MSP430 - Development Tools, ADC - PWM - UART - Timer Interrupts - System design using MSP430Microcontroller.	9
V	**PIC MICROCONTROLLER** CPU Architecture – Instruction set – interrupts- Timers- I2C Interfacing –UART- A/D Converter –PWM and introduction to C-Compilers.	9
	Total Instructional Hours	**45 Hours**

Course Outcome

CO1: To understand the fundamentals of microprocessor architecture.
CO2: To know and appreciate the high performance features in CISC architecture.
CO3: To know and appreciate the high performance features in RISC architecture.
CO4: To perceive the basic features in Motorola microcontrollers.
CO5: To interpret and understand PIC Microcontroller.

TEXT BOOKS:

T1. Daniel Tabak , "Advanced Microprocessors", McGraw Hill.Inc., 1995.
T2. James L. Antonakos , "The Pentium Microprocessor" Pearson Education, 1997.

REFERENCE BOOKS:

R1. Steve Furber, "ARM System – On – Chip architecture", Addision Wesley, 2000.
R2. Andrew N.Sloss, Dominic Symes and Chris Wright "ARM System Developer's Guide : Designing and Optimizing System Software", First edition, Morgan Kaufmann Publishers, 2004.
R3 John. B. Peatman, "Design with PIC Microcontroller", Prentice hall, 1997.

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PROGRAMME	COURSE CODE	NAME OF THE COURSE	L	T	P	C
M.E.	20AE2303	ASIC AND FPGA DESIGN	3	0	0	3

Course Objective

1. Describe the design flow of different types of ASIC and PLD
2. Gain knowledge about floor planning, placement and routing in ASIC
3. Implement the digital design using Verilog and VHDL
4. Infer the architecture of different types of FPGA
5. Describe the design issues of SOC

Unit	Description	Instructional Hours
I	**OVERVIEW OF ASIC AND PLD** Types of ASICs - Design Flow - CAD tools used in ASIC Design - Programming Technologies: Antifuse - Static RAM - EPROM and EEPROM Technology, Programmable Logic Devices: ROMs and EPROMs - PLA - PAL. Gate Arrays - CPLDs and FPGAs	9
II	**ASIC PHYSICAL DESIGN** System partition -Partitioning - Partitioning Methods - Interconnect Delay Models and Measurement of Delay - Floor Planning - Placement - Routing : Global Routing - Detailed Routing - Special Routing - Circuit Extraction - DRC	9
III	**LOGIC SYNTHESIS, SIMULATION AND TESTING** Design Systems - Logic Synthesis - Half Gate ASIC -Schematic Entry - Low Level Design Language - PLA Tools - EDIF- CFI Design Representation. Verilog and Logic Synthesis - VHDL and Logic Synthesis - Types of Simulation - Boundary Scan Test - Fault Simulation - Automatic Test Pattern Generation.	9
IV	**FPGA** Field Programmable Gate Arrays- Logic Blocks, Routing Architecture , FPGA Design : FPGA Physical Design Tools -Technology Mapping - Placement & Routing - Register Transfer (RT) / Logic Synthesis - Controller/Data Path Synthesis - Logic Minimization	9
V	**SOC DESIGN** Design Methodologies – Processes and Flows - Embedded Software Development for SOC - Techniques for SOC Testing – Configurable SOC – Hardware / Software CoDesign - Case studies: Digital Camera, Bluetooth Radio / Modem, SDRAM and USB.	9
	Total Instructional Hours	**45**

Course Outcome

CO1: Summarize the concepts of ASIC and PLD
CO2: Apply the different high performance algorithms in ASICs
CO3: Demonstrate the synthesis, simulation and testing of digital systems
CO4: Outline the different architectures of FPGA
CO5: Discuss the design issues of SOC

TEXT BOOKS:

T1 - David A.Hodges, Analysis and Design of Digital Integrated Circuits ,3rd Edition, Tata Mc Graw Hill , 2004.
T2 - M.J.S. Smith: Application Specific Integrated Circuits, Pearson, 2003.

REFERENCE BOOKS:

R1 - Parag.K.Lala, Digital System Design using Programmable Logic Devices, BSP, 2003.
R2 - Wayne Wolf, FPGA-Based System Design, Prentice Hall PTR, 2004.
R3 - Sudeep Pasricha and NikilDutt, On-Chip Communication Architectures System on Chip Interconnect, Elsevier,2008.
R4 - Farzad Nekoogar and Faranak Nekoogar, From ASICs to SOCs: A Practical Approach, Prentice Hall PTR, 2003.

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PROFESSIONAL ELECTIVE-II

PROGRAMME	COURSE CODE	NAME OF THE COURSE	L	T	P	C
M.E.	20AE2304	COMPUTER ARCHITECTURE AND PARALLEL PROCESSING	3	0	0	3

Course Objective

1. Basic concepts of computer architecture Design and performance.
2. Learn the difference between pipeline and parallel processing concepts.
3. Study Memory Architectures, Memory Technology and Optimization
4. Basic concepts of multiprocessors.
5. Study various types of processor architectures and the importance of scalable architectures

Unit	Description	Instructional Hours
I	**COMPUTER DESIGN AND PERFORMANCE MEASURES** Fundamentals of Computer Design – Parallel and Scalable Architectures – Multiprocessors – Multi-vector and SIMD architectures – Multithreaded architectures – Stanford Dash multiprocessor – KSR1 - Data-flow architectures - Performance Measures.	9
II	**PARALLEL PROCESSING, PIPELINING AND ILP** Instruction Level Parallelism and Its Exploitation - Concepts and Challenges - Pipelining processors -Overcoming Data Hazards with Dynamic Scheduling – Dynamic Branch Prediction - Speculation - Multiple Issue Processors - Performance and Efficiency in Advanced Multiple Issue Processors.	9
III	**MEMORY HIERARCHY DESIGN** Memory Hierarchy - Memory Technology and Optimizations – Cache memory – Optimizations of Cache Performance – Memory Protection and Virtual Memory - Design of Memory Hierarchies.	9
IV	**MULTIPROCESSORS** Symmetric and distributed shared memory architectures – Cache coherence issues – Performance Issues – Synchronization issues – Models of Memory Consistency - Interconnection networks – Buses, crossbar and multi-stage switches.	9
V	**MULTI-CORE ARCHITECTURES** Software and hardware multithreading – SMT and CMP architectures – Design issues – Case-studies – Intel Multi-core architecture – SUN CMP architecture – IBM cell architecture – hp architecture.	9
	Total Instructional Hours	**45**

COURSE OUTCOME

CO1: Design and analysis of computer architecture and performance.
CO2: Learn the difference between pipeline and parallel processing concepts.
CO3: Analysis of Memory Technology and Optimization
CO4: Learn the distribution of shared memory architectures.
CO5: Design and analysis of multi core architecture.

TEXT BOOKS:

T1 David E. Culler, Jaswinder Pal Singh, "Parallel Computing Architecture: A hardware/ software approach", Morgan Kaufmann / Elsevier, 1997

T2 Hwang Briggs, "Computer Architecture and parallel processing", McGraw Hill, 1984.

REFERENCE BOOKS:

R1 John P. Hayes, "Computer Architecture and Organization", McGraw Hill

R2 John P. Shen, "Modern processor design. Fundamentals of super scalar processors", Tata McGraw Hill 2003

R3 Kai Hwang, "Advanced Computer Architecture", McGraw Hill International, 2001

R4 William Stallings, "Computer Organization and Architecture – Designing for Performance", Pearson Education, Seventh Edition, 2006

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PROGRAMME	COURSE CODE	NAME OF THE COURSE	L	T	P	C
M.E.	20AE2305	CAD FOR VLSI DESIGN	3	0	0	3

Course Objective

1. Recall the various physical design methods in VLSI.
2. Understand the concepts behind the VLSI design rules.
3. Infer the concept of floor planning and routing techniques.
4. Interpret the simulation techniques at various levels in VLSI design flow.
5. Illustrate the concepts of various algorithms used for floor planning and routing techniques.

Unit	Description	Instructional Hours
I	**VLSI DESIGN METHODOLOGIES** Introduction to VLSI Design methodologies, Basics of VLSI design automation tools, Algorithmic Graph Theory and Computational Complexity, Tractable and Intractable problems, General purpose methods for combinatorial optimization.	9
II	**DESIGN RULES** Layout Compaction-Design rules-problem formulation-algorithms for constraint graph compaction-placement and partitioning-Circuit representation-Placement algorithms-partitioning	9
III	**FLOOR PLANNING** Floor planning concepts, Shape functions and floorplan sizing, Types of local routing problems, Area routing, Channel routing, Global routing, Algorithms for global routing.	9
IV	**SIMULATION AND LOGIC SYNTHESIS** Simulation, Gate-level modeling and simulation, Switch-level modeling and simulation, Combinational Logic Synthesis, Binary Decision Diagrams, Two Level Logic Synthesis.	9
V	**HIGH LEVEL SYNTHESIS** Hardware models for high level synthesis, internal representation, allocation, assignment and scheduling, scheduling algorithms, Assignment problem, High level transformations.	9
	Total Instructional Hours	**45 Hours**

Course Outcome

CO1: Summarize the various physical design methods in VLSI
CO2: Apply the various VLSI design rules.
CO3: Outline the concept of floor planning and routing
CO4: Demonstrate the concept of Simulation and Logic Synthesis
CO5: Discuss the hardware models for high level synthesis

TEXT BOOKS:

T1. N.A. Sherwani, "Algorithms for VLSI Physical Design Automation", Kluwer Academic Publishers, 2002.
T2. S.H. Gerez, "Algorithms for VLSI Design Automation", John Wiley & Sons, 2002.

REFERENCE BOOKS:

R1. Sadiq M. Sait, Habib Youssef, "VLSI Physical Design automation: Theory and Practice",World Scientific 1999.
R2. Steven M.Rubin, "Computer Aids for VLSI Design", Addison Wesley Publishing 1987.
R3. S.M. Sait and H. Youssef, "VLSI physical design automation: theory and practice", World Scientific Pub. Co., 1999.
R4. D.D. Gajski, N.D. Dutt, A.C. Wu and A.Y. Yin, "High-level synthesis: introduction to chip and system design", Kluwer Academic Publishers, 1992.

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PROGRAMME	COURSE CODE	PROFESSIONAL ELECTIVE-III NAME OF THE COURSE	L	T	P	C
M.E.	20AE2307	ELECTROMAGNETIC INTERFERENCE AND COMPATIBILITY	3	0	0	3

Course Objective

1. Familiarize with the fundamentals that are essential for electronics industry in the field of EMI/EMC
2. Provide knowledge on various EMI sources and victims.
3. Identify the various techniques used in EMC (Electromagnetic compatibility)
4. Design PCB resistant to EMI
5. Provide the various international standards in EMI Measurements

Unit	Description	Instructional hours
I	**EMI/EMC CONCEPTS** EMI-EMC definitions and Units of parameters; Sources and victim of EMI; Conducted and Radiated EMI Emission and Susceptibility; Transient EMI, ESD; Radiation Hazards.	9
II	**EMI COUPLING PRINCIPLES** Sources of Conducted, and radiated interference; Interference coupling by Conduction and Radiation. Common ground impedance coupling ; Common mode and ground loop coupling ; Differential mode coupling ; Power mains and Power supply coupling	9
III	**EMI CONTROL TECHNIQUES** Shielding, Filtering, Grounding, Bonding, Isolation transformer, Transient suppressors, opto isolators, Cable routing, Signal control	9
IV	**PCB DESIGN** Transmitter, Receiver, Antenna,, Power Supply, Motors, Control devices, Digital Circuits, Digital computer Integrated circuit sucessapility	9
V	**EMI MEASUREMENTS AND STANDARDS** Open area test site; TEM cell; EMI test shielded chamber and shielded ferrite lined anechoic chamber; Tx /Rx Antennas, Working Principles of EMI sensing Device; EMI Rx and spectrum analyzer; Civilian standards-CISPR, FCC, IEC, EN; Military standards-MIL461E/462.	9
	Total instructional hours	**45**

Course Outcome

CO1: Real world EMC deigns constraints and to achieve the most cost effective design that meets all requirements.
CO2: Diagnose and solve the basic electromagnetic compatibility problems.
CO3: Designing the electronic system that function without errors or problems that are related to electromagnetic compatibility.
CO4: Measuring the EMI with various methods and comparing it with standards.
CO5: Controlling techniques for EMI and EMC.

TEXT BOOKS:

T1. V.P.Kodali, "Engineering EMC Principles, Measurements and Technologies", IEEE Press, Newyork, 1996.
T2. S.Sathyamurthy "Basics of Electromagnetic Compatibility "sams publishers ,2008.

REFERENCE BOOKS:

R1. Henry W.Ott.,"Noise Reduction Techniques in Electronic Systems", A Wiley Inter Science, 1992.
R2. Bemhard Keiser, "Principles of Electromagnetic Compatibility", 3rd Ed, Artech house, 2008.
R3. C.R.Paul,"Introduction to Electromagnetic Compatibility" , John Wiley and Sons, Inc, 1992.
R4. Don R.J.White Consultant Incorporate, "Handbook of EMI/EMC", Vol I-V, 1988

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PROGRAMME	COURSE CODE	NAME OF THE COURSE	L	T	P	C
M.E.	20AE2308	WIRELESS ADHOC AND SENSOR NETWORKS	3	0	0	3

Course Objectives

1. To understand the basics of Ad-hoc & Sensor Networks.
2. To learn various fundamental and emerging protocols of all layers
3. To study about the issues pertaining to major obstacles in establishment and efficient management of Ad-hoc and sensor networks.
4. To understand the nature and applications of Ad-hoc and sensor networks.
5. To understand various security practices and protocols of Ad-hoc and Sensor Networks.

Unit	Description	Instructional Hours
I	**MAC & TCP IN AD HOC NETWORKS** Fundamentals of WLANs – IEEE 802.11 Architecture - Self configuration and Auto configuration-Issues in Ad-Hoc Wireless Networks – MAC Protocols for Ad-Hoc Wireless Networks – Contention Based Protocols - TCP over Ad-Hoc networks-TCP protocol overview - TCP and MANETs – Solutions for TCP over Ad-Hoc Networks.	9
II	**ROUTING IN AD HOC NETWORKS** Routing in Ad-Hoc Networks- Introduction-Topology based versus Position based Approaches-Proactive, Reactive, Hybrid Routing Approach-Principles and issues – Location services - DREAM – Quorums based location service – Grid – Forwarding strategies – Greedy packet forwarding – Restricted directional flooding- Hierarchical Routing- Issues and Challenges in providing QoS.	9
III	**MAC, ROUTING & QOS IN WIRELESS SENSOR NETWORKS** Introduction – Architecture - Single node architecture – Sensor network design considerations – Energy Efficient Design principles for WSNs – Protocols for WSN – Physical Layer : Transceiver Design considerations – MAC Layer Protocols – IEEE 802.15.4 Zigbee – Link Layer and Error Control issues - Routing Protocols – Mobile Nodes and Mobile Robots - Data Centric & Contention Based Networking – Transport Protocols & QOS – Congestion Control issues – Application Layer support	9
IV	**SENSOR MANAGEMENT** Sensor Management - Topology Control Protocols and Sensing Mode Selection Protocols - Time synchronization - Localization and positioning – Operating systems and Sensor Network programming – Sensor Network Simulators.	9
V	**SECURITY IN AD HOC AND SENSOR NETWORKS** Security in Ad-Hoc and Sensor networks – Key Distribution and Management – Software based Anti-tamper techniques – water marking techniques – Defense against routing attacks - Secure Adhoc routing protocols – Broadcast authentication WSN protocols – TESLA – Biba – Sensor Network Security Protocols – SPINS	9
	Total Instructional Hours	**45**

Course Outcomes

- CO1 Identify different issues in wireless ad hoc and sensor networks.
- CO2 Analyze protocols developed for ad hoc and sensor networks.
- CO3 Identify and address the security threats in ad hoc and sensor
- CO4 Establish a Sensor network environment for different type of applications.
- CO5 Understand the security in Ad hoc and Sensor networks

TEXT BOOKS:

T1 C.Siva Ram Murthy and B.S.Manoj, "Ad Hoc Wireless Networks – Architectures and Protocols", Pearson Education, 2004.

T2 Waltenegus Dargie, Christian Poellabauer, "Fundamentals of Wireless Sensor Networks Theory and Practice", John Wiley and Sons, 2010.

REFERENCE BOOKS:

R1 Carlos De Morais Cordeiro, Dharma Prakash Agrawal "Ad Hoc and Sensor Networks: Theory and Applications (2nd Edition), World Scientific Publishing, 2011.

R2 C.K.Toh, "Ad Hoc Mobile Wireless Networks", Pearson Education, 2002.

R3 Holger Karl, Andrea's willig, "Protocols and Architectures for Wireless Sensor Networks, John Wiley & Sons, Inc .2005.

R4 Subir Kumar Sarkar, T G Basavaraju, C Puttamadappa, "Ad Hoc Mobile Wireless Networks", Auerbach Publications, 2008.

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PROGRAMME	COURSE CODE	NAME OF THE COURSE	L	T	P	C
M.E.	20AE2309	ROBOTICS AND INTELLIGENT SYSTEMS	3	0	0	3

Course Objectives

1 To Teach the basic concepts in robotics.
2 To expose the various design aspects in robot grippers.
3 To make learn various drives and control systems.
4 To impart knowledge on machine vision systems.
5 To apply robot based concepts for automation

Unit	Description	Instructional Hours
I	**INTRODUCTION** Basic Concepts such as Definition, three laws, DOF, Misunderstood devices etc., Elements of Robotic Systems i.e. Robot anatomy, Classification, Associated parameters i.e. resolution, accuracy, repeatability, dexterity, compliance, RCC device, etc. Automation-Concept, Need, Automation in Production System, Principles and Strategies of Automation, Basic Elements of an Automated System, Advanced Automation Functions, Levels of Automations, introduction to automation productivity.	9
II	**ROBOT GRIPPERS** Types of Grippers, Design aspect for gripper, Force analysis for various basic gripper system. Sensors for Robots:- Characteristics of sensing devices, Selections of sensors, Classification and applications of sensors. Types of Sensors, Need for sensors and vision system in the working and control of a robot.	9
III	**DRIVES AND CONTROL SYSTEMS** Types of Drives, Actuators and its selection while designing a robot system. Types of transmission systems, Control Systems -Types of Controllers, Introduction to closed loop control .Control Technologies in Automation:- Industrial Control Systems, Process Industries Verses Discrete-Manufacturing Industries, Continuous Verses Discrete Control, Computer Process and its Forms. Control System Components such as Sensors, Actuators and others.	9
IV	**MACHINE VISION SYSTEM** Vision System Devices, Robot Programming: - Methods of robot programming, lead through programming, motion interpolation, branching capabilities, WAIT, SIGNAL and DELAY commands, subroutines, Programming Languages: Introduction to various types such as RAIL and VAL II etc, Features of type and development of languages for recent robot systems.	9
V	**MODELING AND SIMULATION FOR MANUFACTURING PLANT AUTOMATION** Introduction, need for system Modeling, Building Mathematical Model of a manufacturing Plant,Modern Tools- Artificial neural networks in manufacturing automation, AI in manufacturing,Fuzzy decision and control, robots and application of robots for automation.Artificial Intelligence:- Introduction to Artificial Intelligence, AI techniques, Need and application of AI. Other Topics in Robotics:- Socio-Economic aspect of robotisation. Economical aspects for robot design, Safety for robot and associated mass, New Trends & recent updates in robotics.	9
	Total Instructional Hours	**45**

Course Outcomes

CO1 Ability to implement simple concepts associated with Robotics and Automation
CO2 Ability to use various Robotic sub-systems
CO3 Ability to use kinematics and dynamics to design exact working pattern of robots
CO4 Ability to implement computer vison algorithms for robots
CO5 Be aware of the associated recent updates in Robotics

TEXT BOOKS:

T1 John J. Craig," Introduction to Robotics (Mechanics and Control)", Addison-Wesley, 2nd Edition, 2004
T2 Mikell P. Groover et. Al., "Industrial Robotics: Technology, Programming and Applications", McGraw – Hill International, 1986

REFERENCE BOOKS:

R1 Shimon Y. Nof , "Handbook of Industrial Robotics" , John Wiley Co,2001.
R2 Automation, "Production Systems and Computer Integrated Manufacturing", M.P. Groover, Pearson Education.
R3 Richard D. Klafter , Thomas A. Chemielewski, Michael Negin, "Robotic Engineering : An Integrated Approach" , Prentice Hall India, 2002.
R4 R.C. Dorf, "Handbook of design, manufacturing & Automation" John Wiley and Sons.

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SYLLABUS

SEMESTER III

PROGRAMME	COURSE CODE	NAME OF THE COURSE	L	T	P	C
M.E.	16AP3201	COMPUTER ARCHITECTURE AND PARALLEL PROCESSING	3	0	0	3

Course Objective

1. Compare the performance of various computer architectures.
2. Discriminate between the various data processing architectures.
3. Infer memory technology and measure its performances.
4. Describe the performance of various multiprocessor architectures.
5. Analysis of various multi core architectures.

Unit	Description	Instructional Hours
I	**COMPUTER DESIGN AND PERFORMANCE MEASURES** Concepts of Computer Design – Parallel and Scalable Architectures –Multiprocessors –Multivector and SIMD architectures - Multi threaded architectures – Data-flow architectures - Performance Measures.	9
II	**PARALLEL PROCESSING, PIPELINING AND ILP** Instruction Level Parallelism and Its Exploitation - Concepts and Challenges –Overcoming Data Hazard with Dynamic Scheduling Dynamic Branch Prediction - Speculation - Multiple Issue Processors - Performance and Efficiency in Advanced Multiple Issue Processors.	9
III	**MEMORY HIERARCHY DESIGN** Memory Hierarchy - Memory Technology and Optimizations – Cache memory – Optimizations of Cache Performance –Memory Protection and Virtual Memory -Design of Memory Hierarchies.	9
IV	**MULTIPROCESSOR** Symmetric and distributed shared memory architectures –Cache coherence issues – Performance Issues – Synchronization issues – Models of Memory Consistency -Interconnection networks – Buses, crossbar and multistage switches.	9
V	**MULTI-CORE ARCHITECTURES** Software and hardware multithreading – SMT and CMP architectures – Design issues –Case studies – Intel Multi-core architecture ARM processor Multicore architecture – BUS protocol for Multicore architecture.	9
	Total Instructional Hours	**45**

Course outcome

CO1: Categorize the performance of various architectures.
CO2: Prioritize the best performing architectures.
CO3: Design memories under various hierarchies.
CO4: Estimate the performance of various multiprocessor architectures.
CO5: Choose the suitable multi core architecture based on the applications.

TEXT BOOKS:

T1. Kai Hwang, "Advanced Computer Architecture", McGraw Hill International, 2001.
T2. John L. Hennessey and David A. Patterson, "Computer Architecture – A quantitative approach", Morgan Kaufmann / Elsevier, 4th Edition, 2007.

REFERENCE BOOKS:

R1. David E. Culler, Jaswinder Pal Singh, "Parallel Computing Architecture: A hardware/ software Approach", Morgan Kaufmann / Elsevier, 1997.
R2. John P. Shen, "Modern processor design. Fundamentals of super scalar processors", Tata McGraw Hill 2003.
R3. William Stallings, "Computer Organization and Architecture Designing for Performance", Pearson Education, Seventh Edition, 2006.

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PROGRAMME	COURSE CODE	NAME OF THE COURSE	L	T	P	C
M.E.	16AP3001	ELECTRONICS SYSTEM DESIGN LABORATORY	0	0	4	2

Course Objective

1. Impart the knowledge on various analog / digital transceiver systems and control different process.
2. Design system using 8086 and 8051 Microcontroller.
3. Study the different interfaces using Embedded Microcontroller.
4. Intend and analysis of real time signal processing system.
5. Identify and design advanced electronics system (Analog and Digital Systems) and conduct experiments, analyze and interpret data.

Expt. No.	Description of the experiments
1	System design using PIC, MSP430, '51 Microcontroller and 16- bit Microprocessor - 8086.
2	Study of different interfaces (using Embedded Microcontroller).
3	Implementation of Adaptive Filters and multistage multirate system in DSP Processor.
4	Simulation of QMF using Simulation Packages.
5	Analysis of Asynchronous and clocked synchronous sequential circuits.
6	Built in self test and fault diagnosis.
7	Sensor design using simulation tools.
8	Design and analysis of real time signal processing system-Data acquisition and signal Processing.

Total Practical Hours 45

Course Outcome

CO1: Design various analog / digital transceiver systems and control different process.
CO2: Write programs in Xilinx Microcontroller (8051) and DSP processor.
CO3: Analyze Synchronous and Asynchronous sequential circuits.
CO4: Propose interfaces using embedded Microcontroller.
CO5: Design and analysis of real time signal processing system.

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PROGRAMME	COURSE CODE	NAME OF THE COURSE	L	T	P	C
M.E.	16AP3901	PROJECT PHASE - I	0	0	12	6

Course Objective

1. Analyze a methodology to select a project and able to develop a hardware/software project.
2. Transform the ideas behind the project with clarity.
3. Validate the technical report.

Description of the project work

A candidate is permitted to work on projects in an Industrial / Research Organization, on the recommendations of the Head of the Department concerned.

A project must be selected either from research literature published list or the students themselves may propose suitable topics in consultation with their guide.

The aim of the project work is to strengthen the comprehension of principles by applying them to a new problem which may be the design and manufacture of a device, a research investigation or a design problem.

The project work shall be supervised by a supervisor of the department, (and an expert in industry if it is a industrial project), and the student shall be instructed to meet the supervisor periodically and to attend the review committee meeting for evaluation of the progress.

In case of candidates not completing Phase-I of project work successfully, the candidates can undertake Phase-I again in the subsequent semester. In such cases the candidates can enroll for Phase-II, only after successful completion of Phase-I.

The Project report shall be prepared and submitted according to the approved guidelines as given by the Controller of Examination and bonafied duly signed by Supervisor and the Head of the Department.

Course Outcome

CO1: Realize the skills acquired in the previous semesters to solve complex engineering problems.
CO2: Build up an innovative model / prototype of an idea related to the field of specialization.
CO3: Create the work individually to identify, troubleshoot and build products for environmental and societal issues.
CO4: Effective presentation of ideas with clarity.
CO5: Evaluate surveys towards developing a product which helps in life time learning.

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SEMESTER IV

PROGRAMME	COURSE CODE	NAME OF THE COURSE	L	T	P	C
M.E.	16AP4902	PROJECT PHASE - II	0	0	24	12

Course Objective

1. Analyze a methodology to select a project and able to develop a hardware/software project.
2. Transform the ideas behind the project with clarity.
3. Validate the technical report.

Description of the project work

The Project work (Phase II) shall be pursued for a minimum prescribed period as per regulation.

The project work shall be supervised by a supervisor of the department, (and an expert in industry if it is a industrial project), and the student shall be instructed to meet the supervisor periodically and to attend the review committee meeting for evaluation of the progress.

The Project report shall be prepared and submitted according to the approved guidelines as given by the Controller of Examination and bonafied duly signed by Supervisor and the Head of the Department.

Course Outcome

CO1: Realize the skills acquired in the previous semesters to solve complex engineering problems.
CO2: Build up an innovative model / prototype of an idea related to the field of specialization.
CO3: Create the work individually to identify, troubleshoot and build products for environmental and societal issues.
CO4: Effective presentation of ideas with clarity.
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PROFESSIONAL ELECTIVE V

PROGRAMME	COURSE CODE	NAME OF THE COURSE	L	T	P	C
M.E.	16AP3301	TESTING OF VLSI CIRCUITS	3	0	0	3

Course Objective

1. Infer basic concepts on testing of VLSI circuits.
2. Recall the basics of combinational and sequential circuits.
3. Gain knowledge on testing of logic circuits.
4. Learn algorithms for testing the logical circuits.
5. Diagnose the faults in combinational and logic circuits.

Unit	Description	Instructional Hours
I	**TESTING AND FAULT MODELLING** Introduction to testing – Faults in Digital Circuits – Modelling of faults – Logical Fault Models – Fault detection – Fault Location – Fault dominance – Logic simulation – Types of simulation – Delay models – Gate Level Event – driven simulation.	9
II	**TEST GENERATION FOR COMBINATIONAL AND SEQUENTIAL CIRCUITS** Test generation for combinational logic circuits – Testable combinational logic circuit design – Test generation for sequential circuits – design of testable sequential circuits.	9
III	**DESIGN FOR TESTABILITY** Design for Testability – Ad-hoc design – Generic scan based design – Classical scan based design – System level DFT approaches.	9
IV	**SELF – TEST AND TEST ALGORITHMS** Built-In self Test – Test pattern generation for BIST – Circular BIST – BIST Architectures – Testable Memory Design – Test Algorithms – Test generation for Embedded RAMs.	9
V	**FAULT DIAGNOSIS** Logical Level Diagnosis – Diagnosis by UUT reduction – Fault Diagnosis for Combinational Circuits – Self-checking design – System Level Diagnosis.	9
	Total Instructional Hours	**45**

Course Outcome

CO1: Design models of various fault diagnosis circuits.
CO2: Construct test circuit for combinational and sequential processes.
CO3: Analyze the various test generation methods for logic circuits.
CO4: Employ the appropriate design algorithm for constructing logic circuits.
CO5: Suggest suitable circuit for fault diagnosis.

TEXT BOOKS:

T1. M.Abramovici, M.A.Breuer and A.D. Friedman, "Digital systems and Testable Design", Jaico Publishing House, 2002.
T2. P.K. Lala, "Digital Circuit Testing and Testability", Academic Press, 2002.

REFERENCE BOOKS:

R1. M.L.Bushnell and V.D.Agrawal, "Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits", Kluwer Academic Publishers, 2002.
R2. A.L.Crouch, "Design Test for Digital IC's and Embedded Core Systems", Prentice Hall International, 2002.

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PROGRAMME	COURSE CODE	NAME OF THE COURSE	L	T	P	C
M.E.	16AP3302	PHOTONICS	3	0	0	3

Course Objective

1. Gain knowledge on light and its propagation.
2. Analyze the performance of bistable LASER diodes.
3. Distinguish the performance issues in LASER diodes.
4. Design electronic circuits for wavelength selection and photo detection.
5. Propose suitable applications for photonic switching.

Unit	Description	Instructional Hours
I	**INTRODUCTION** Function semiconductor laser - Basic concepts of semi conductor laser - Semi conductor quantum wells - Vertical cavity surface emitting lasers - Non linear effects in semiconductor lasers.	9
II	**BISTABLE LASER DIODES** Optical Bistability - Bistable switches - Inhomogeneous current injections – absorptive scheme - Dispersive bistable laser diodes - Injection locking - Bistability in laser diode amplifiers - wavelength, power and polarization bistability.	9
III	**SELF PULSATION & ULTRA SHORT PULSE GENERATORS** Self pulsation-theory of self pulsation in laser diodes, Period doubling in modulated laser diodes - Optical chaos - Mode locking in laser diodes - Monolithic mode locked laser diodes.	9
IV	**WAVELENGTH SELECTION AND WAVELENGTH SELECTIVE PHOTODETECTION** Wavelength selection - Laser diode amplifier filters - DFB laser diode amplifier - Signal selection, Noise properties and Wavelength selection photo detectors.	9
V	**APPLICATIONS OF PHOTONIC SWITCHING** High speed data transmission systems - Clock distribution - All optical fibre communication systems - Clock extraction & dispersion compensation - WDM systems - optical exchange systems - Time division & wavelength division switching - Power mixing & Frequency division switching - Space switches.	9
	Total Instructional Hours	**45**

Course Outcome

CO1: Elaborate the performance issues in various LASERS.
CO2: Suggest suitable application for bistable LASER diodes.
CO3: Appraise the solutions for the performance issues in LASER diodes.
CO4: Adapt the suitable circuit for wavelength selection, detection and photo detection.
CO5: Evaluate the applications of photonic switching.

TEXT BOOKS:

T1. H. Kawaguchi, "Bistabilities and Non-linearities in Laser Diodes", Artech house Inc, Norwood, 1994.
T2. Saleh, B. E. A., and M. C. Teich., "Fundamentals of Photonics", New York, NY: Wiley, 1991.

REFERENCE BOOKS:

R1. Sueta and Okoshi, "Fundamental of Ultra fast & Ultra Parallel Opto Electronics", John Wiley & Sons, New York, 1996.
R2. K. Tada and Hinton. H.S,, "Photonic Switching II", Springer Verlag, Berlin, 1990.

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PROGRAMME	COURSE CODE	NAME OF THE COURSE	L	T	P	C
M.E.	16AP3303	NANO ELECTRONICS	3	0	0	3

Course Objective

1. Learn the basics of various dimensional nanostructures.
2. Analyze various properties of nanostructure.
3. Understand the importance of quantum dots in nano structures.
4. Infer the basics of nano structure devices.
5. Design application circuits using nano structures.

Unit	Description	Instructional Hours
I	**INTRODUCTION** Electronic states in crystal energy bands - 1 D nanostructures (quantum wires) - OD nanostructures (quantum dots) - Concepts of 2 and 3D nanostructures (quantum wells), artificial atomic clusters.	9
II	**FABRICATION AND MEASUREMENT TECHNIQUES** Size dependent properties - Size dependent absorption spectra - Blue shift with smaller sizes - Phonons in nanostructures - Contacts at Nano level – AFM (classification) - lSTM tip on a surface.	9
III	**PROPERTIES** Charging of quantum dots - Coulomb blockade - Quantum mechanical treatment of quantum wells - wires and dots - Widening of band gap in quantum dots - Strong and weak confinement - Properties of coupled quantum dots - Optical scattering from Nano defects.	9
IV	**NANO STRUCTURE DEVICES** Nano composites – Ceramic - Polymer and metal material composites - Electronic and atomic structure of aggregates and nano particles - Theory and modeling of nano particles fictionalization processes - organic electronics.	9
V	**LOGIC DEVICES AND APPLICATIONS** Nano systems -Synthesis and characterization methods - Molecular beam epitaxy - MOCVD - chemical routes - nano particles of polymers - pulsed laser deposition - ion beam assisted techniques including embedded nano particles - RF sputtering. -Inert gas condensation.	9
	Total Instructional Hours	**45**

Course Outcome

CO1: Summarize the concepts on various dimensional nanostructures.
CO2: Compile the properties of nanostructure.
CO3: Recognize the basics of nanostructure devices and logic devices.
CO4: Compile the performance of nano structure devices.
CO5: Categories the application circuits of nano structures.

TEXT BOOKS:

T1. K.Bamam and D.Vvedensky "Low Dimensional Semiconductor Structures", Cambridge University Book, 2001.
T2. L.Banyai and S.W.Koch, "Semiconductor Quantum Dots", World Scientific, 1993.

REFERENCE BOOKS:

R1. J.H. Davies, "An introduction to the physics-a low dimensional semiconductors", Cambridge Press, 1998.
R2. Karl Goser, Peter Glosekotter, Jan Dienstuhl., "Nanoelectronics and Nanosystems", Springer, 2004.

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PROGRAMME	COURSE CODE	NAME OF THE COURSE	L	T	P	C
M.E.	16AP3304	INTERNETWORKING AND MULTIMEDIA	3	0	0	3

Course Objective

1. Identify and analyze the requirements of multimedia communication network.
2. Infer the basics of broad band technology.
3. Learn the basics of reliable transport protocols.
4. Infer about various multimedia communication standards and architectures.
5. Analyze the process involved in data transmission across various networks.

Unit	Description	Instructional Hours
I	**MULTIMEDIA NETWORKING** Digital Sound, Video and Graphics – Basic Multimedia Networking – Multimedia Characteristics – Evolution of Internet Services Model – Network Requirements for Audio/ Video Transform – Multimedia Coding and Compression for Text, Image Audio And Video.	9
II	**BROADBAND NETWORK TECHNOLOGY** Broadband Services – ATM and IP, IPV6, High Speed Switching – Resource Reservation - Buffer Management – Traffic Shaping – Caching – Scheduling and Policing – Throughput - Delay and Jitter Performance – Storage and Media Services – Voice and Video over IP – MPEG–2 over ATM/IP – Indexing Synchronization of Requests – Recording and Remote Control .	9
III	**RELIABLE TRANSPORT PROTOCOL AND APPLICATIONS** Multicast over Shared Media Network – Multicast Routing and Addressing – Scaling Multicast and NBMA Networks – Reliable Transport Protocols – TCP Adaptation Algorithm – RTP - RTCP – MIME – Peer–to–Peer Computing – Shared Application – SIP - SDP.	9
IV	**MULTIMEDIA COMMUNICATION STANDARDS** Objective of MPEG – 7 Standards – Functionalities and Systems of MPEG–7 MPEG–21 Multimedia Framework Architecture – Content Representation – Content Management and Usage – Intellectual Property Management – Audio Visual System – H264: Guaranteed QOS LAN Systems – MPEG_4 Video Transport Across Internet.	9
V	**MULTIMEDIA COMMUNICATION ACROSS NETWORKS** Packet Audio/Video in The Network Environment –Video Transport Across Generic Networks – Layered Video Coding– Error Resilient Video Coding Techniques – Scalable Rate Control – Streaming Video Across Internet – Multimedia Transport Across ATM Networks and IP Network – Multimedia Across Wireless Networks .	9
	Total Instructional Hours	**45**

Course Outcome

CO1: Describe different realizations of multimedia tools and the way in which they are used.
CO2: Summarize the structure of broad band techniques and its associated standards.
CO3: Design a suitable application using reliable transport protocols.
CO4: Compare and contrast different multimedia standards.
CO5: Discuss the data transfer process across various networks.

TEXT BOOKS:

T1. B. O. Szuprowicz, "Multimedia Networking", McGraw Hill, Newyork, 1995.
T2. K. R. Rao, Zoran S, Bojkovic and Dragorad A, Milovanovic "Multimedia communication systems", PHI, 2003.

REFERENCE BOOKS:

R1. Jon Crowcroft, Mark Handley, Ian Wakeman "Internetworking Multimedia" Harcourt, Singapore, 1998.
R2. Tay Vaughan, "Multimedia making it to work", 4th edition Tata McGraw Hill, New Delhi, 2000.

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PROGRAMME	COURSE CODE	NAME OF THE COURSE	L	T	P	C
M.E.	16AP3305	ASIC DESIGN	3	0	0	3

Course Objective

1. Study the design flow of different types of ASIC.
2. Discuss the architecture of ASIC.
3. Gain knowledge on partitioning, floor planning, placement and routing including circuit extraction of ASIC.
4. Learn about different high performance algorithms and its applications in ASICs.
5. Infer about the partitioning and routing methods in ASIC circuits.

Unit	Description	Instructional Hours
	INTRODUCTION TO ASICS, CMOS LOGIC AND ASIC LIBRARY DESIGN	
I	Types of ASICs - Design flow - CMOS transistors CMOS Design rules – Combinational Logic Cell – Sequential logic cell - Data path logic cell - Transistors as Resistors - Transistor Parasitic Capacitance- Logical effort –Library cell design - Library architecture.	9
	PROGRAMMABLE ASICS, PROGRAMMABLE ASIC LOGIC CELLS	
II	AND programmable ASIC I/O cells anti fuse - static RAM - EPROM and EEPROM technology - PREP benchmarks - Actel ACT - Xilinx LCA –Altera FLEX - Altera MAX DC & AC inputs and outputs - Clock & Power inputs - Xilinx I/O blocks.	9
	PROGRAMMABLE ASIC INTERCONNECT, PROGRAMMABLE ASIC DESIGN SOFTWARE AND LOW LEVEL DESIGN ENTRY	
III	Actel ACT -Xilinx LCA - Xilinx EPLD - Altera MAX 5000 and 7000 - Altera MAX 9000 - Altera FLEX –Design systems - Logic Synthesis - Half gate ASIC -Schematic entry – Low level design language - PLA tools -EDIF- CFI design representation.	9
	LOGIC SYNTHESIS, SIMULATION AND TESTING	
IV	Verilog and logic synthesis -VHDL and logic synthesis - Types of simulation –Boundary scan test - fault simulation - Automatic test pattern generation.	9
	ASIC CONSTRUCTION, FLOOR PLANNING, PLACEMENT AND ROUTING	
V	System partition - FPGA partitioning - partitioning methods - floor planning - placement - physical design flow –global routing - detailed routing - special routing - circuit extraction - DRC.	9
	Total Instructional Hours	**45**

Course Outcome

CO1: Analyze the characteristics and performance of ASICs and judge independently the best suited device for fabrication.
CO2: Conducting research in ASIC design.
CO3: Solve design issues and simulate and Test ASICs.
CO4: Apply appropriate techniques, resources and tools to develop ASICs for engineering activities
CO5: Design the ASIC circuit.

TEXT BOOKS:

T1. M.J.S .Smith, "Application Specific Integrated Circuits", Addison -Wesley Longman Inc., 1997.
T2. Farzad Nekoogar and Faranak Nekoogar, "From ASICs to SOCs: A Practical Approach", Prentice Hall PTR, 2003.

REFERENCE BOOKS:

R1. Wayne Wolf, "FPGA-Based System Design", Prentice Hall PTR, 2004.
R2. Rajsuman, "System-on-a-Chip Design and Test", Santa Clara, CA: Artech House Publishers, 2000.
R3 F. Nekoogar, "Timing Verification of Application-Specific Integrated Circuits (ASICs)", Prentice Hall PTR, 1999.

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PROFESSIONAL ELECTIVE VI

PROGRAMME	COURSE CODE	NAME OF THE COURSE	L	T	P	C
M.E.	16AP3306	ROBOTICS	3	0	0	3

Course Objective

1. Infer the fundamentals of robotics.
2. Recall the concepts of vision system.
3. Outline the working of sensor devices.
4. Coding for developing robot using artificial intelligence techniques.
5. Apply artificial intelligence algorithms to design robots.

Unit	Description	Instructional Hours
I	**INTRODUCTION** Robotic Classification, Robot Specifications, Motion – Bug and tangent algorithms, Potential Function, Road maps- Topological roadmaps, Cell decomposition – Trapezoidal and Morse cell decompositions, Sensor and sensor planning- Kinematics-Forward and Inverse Kinematics - Transformation matrix and DH transformation-Inverse Kinematics - Geometric methods and Algebraic methods.	9
II	**COMPUTER VISION** Projection – Optics - Projection on the Image Plane and Radiometry. - Image Processing – Connectivity - Images-Gray Scale and Binary Images - Blob Filling - Thresholding, Histogram-Convolution - Digital Convolution and Filtering and Masking Techniques- Edge Detection - Mono and Stereo Vision.	9
III	**SENSORS AND SENSING DEVICES** Introduction to various types of sensor- Resistive sensors. Range sensors - LADAR (Laser Distance and Ranging), Sonar, Radar and Infra-red- Introduction to sensing - Light sensing, Heat sensing, touch sensing and Position calculating by using mono-vision camera.	9
IV	**ARTIFICIAL INTELLIGENCE** Uniform Search strategies - Breadth first - Depth first - Depth limited - Iterative and deepening depth first search and Bidirectional search - algorithm- Planning - State-Space Planning Plan-Space Planning - Graph plan/Sat Plan and their Comparison - Multi-agent planning and Multi-agent planning - Probabilistic Reasoning - Bayesian Networks - Decision Trees and Bayes net inference.	9
V	**INTEGRATION TO ROBOT** Building of 4 axis or 6 axis robot - Vision System for pattern detection - Sensors for obstacle detection - AI algorithms for path finding and decision making.	9
	Total Instructional Hours	**45**

Course Outcome

CO1: Illustrate the fundamentals of robots.
CO2: Compile the concepts learnt about robotic vision system.
CO3: Develop robots with differential motion and control.
CO4: Build programs for robots in various applications.
CO5: Identify the robotic applications with various axes.

TEXT BOOKS:

T1. Duda, Hart and Stork, "Pattern Recognition", Wiley-Inter science, 2000.

T2. Mallot, "Computational Vision: Information Processing in Perception and Visual Behavior", Cambridge, 2000.

REFERENCE BOOKS:

R1. Stuart Russell and Peter Norvig, "Artificial Intelligence-A Modern Approach", Pearson Education Series in Artificial Intelligence, 2004.

R2. Robert Schilling and Craig, "Fundamentals of Robotics: Analysis and Control", Hall of India Private Limited, 2003.

R3 Forsyth and Ponce, "Computer Vision: A Modern Approach", Person Education, 2003.

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PROGRAMME	COURSE CODE	NAME OF THE COURSE	L	T	P	C
M.E.	16AP3307	MEMS AND NEMS	3	0	0	3

Course Objective

1. Learn the basics of micro electromechanical devices.
2. Infer the fabrication process of Microsystems.
3. Design MEMS sensor.
4. Discuss about scaling and packaging issues in MEMS.
5. Intend suitable application for MEMS.

Unit	Description	Instructional Hours
I	**OVERVIEW AND INTRODUCTION** MEMS and NEMS – working principles - MEMS processes & features, various components of MEMS, applications and standards, micromachining, basic process tools – epitaxy – sputtering - chemical vapor deposition and spin on methods – oxidation –evaporation - lithography and etching - advanced process tools - sol gel process - EFAB.	9
II	**MATERIALS FOR MEMS AND ENGINEERING ASPECTS** Silicon - Silicon oxide and nitride - Thin metal films – Polymers - Other materials and substrates - polycrystalline materials - mechanics of Microsystems - static bending -mechanical vibrations - thermo mechanics - fracture mechanism – fatigue - and stress and strain - young's modulus and modulus of rigidity - scaling laws in miniaturization.	9
III	**MEMS SENSORS, DESIGN AND PROCESSING** Micro sensors (acoustic wave sensors- biomedical sensors- chemical sensors- optical sensors- capacitive sensors- pressure sensors- thermal sensors) - micro actuators (thermal- piezoelectric- electrostatic actuators- micrometers- micro valves & pumps- accelerometer- micro fluidics and devices) - design consideration - process design and mechanical design.	9
IV	**MEMS/NEMS SCALING ISSUES AND PACKAGING** Introduction – Scaling of physical systems – Mechanical system scaling, Thermal system scaling - Fluidic system scaling - Electrical system scaling - Packaging - mechanical and micro system package - design considerations - Process steps - Die preparation – interconnects - surface and Wafer bonding - wire bonding and scaling - 3D packaging and assembly signal Thermal management - Hermetic packaging, Electrical / Micro fluidic / and optical interconnects - Signal mapping transduction - Micro fluidic technology - MEMS and NEMS technology for micro fluidic devices.	9
V	**MEMS/NEMS APPLICATIONS** Applications in automotive industry – health care – aerospace – industrial product consumer products – lab on chip – molecular machines – data storage devices – micro reactor – telecommunications - Servo systems.	9
	Total Instructional Hours	**45**

Course Outcome

CO1: Illustrate the fundamentals of MEMS.
CO2: Describe the materials used for MEMS.
CO3: Design and analysis of MEMS sensors and actuators.
CO4: Summarize MEMS / NEMS scaling issues and packaging.
CO5: Analysis the applications of MEMS.

TEXT BOOKS:

T1. Nadim Malut and Kirt Williams, "An introduction to Micro electro mechanical systems Engineering", Artech House Inc, Boston, Second edition, 2004.

T2. James J Allen, "Micro electro mechanical systems Design", CRC Press, Taylor and Francis Group, 2001.

REFERENCE BOOKS:

R1. Nicolae Lobontiu and Ephrahim Garcia Kluwer, "Mechanics of micro electro mechanical systems", Academic Publishers, Boston, 2001.

R2. Ivor Brodie and Julius J.Muray, "The Physics of Micro/Nano – Fabrication", Springer Science & Business Media, 2013.

R3 Kaoru Ohno, Masatoshi Tanaka, Jun Takeda and Yoshijuki Kawazoe, "Nano - and Micromaterials", Springer Science & Business Media, 2008.

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PROGRAMME	COURSE CODE	NAME OF THE COURSE	L	T	P	C
M.E.	16AP3308	SYSTEM ON CHIP DESIGN	3	0	0	3

Course Objective

1. Learn about designing various logic gates with minimum size, spacing, and parasitic values.
2. Design combinational logic functions and analyze delay and testability properties of interconnect and gates.
3. Correlate optimization of power in sequential logic machines.
4. Study the design principles of FPGA and PLA.
5. Learn various floor planning methods for system design.

Unit	Description	Instructional Hours
I	**LOGIC GATES** Introduction- Combinational Logic Functions- Static Complementary Gates- Switch Logic- Alternative Gate Circuits- Low - Power Gates- Delay Through Resistive Interconnect - Delay Through Inductive Interconnect.	9
II	**COMBINATIONAL LOGIC NETWORKS** Introduction- Standard Cell - Based Layout- Simulation- Combinational Network Delay- Logic and interconnect Design- Power Optimization- Switch Logic Networks- Combinational Logic Testing.	9
III	**SEQUENTIAL MACHINES** Introduction- Latches and Flip - Flops- Sequential Systems and Clocking Disciplines- Sequential System Design- Power Optimization- Design Validation- Sequential Testing.	9
IV	**SUBSYSTEM DESIGN** Introduction- Subsystem Design Principles- Combinational Shifters- Adders- ALUs- Multipliers- High - Density Memory- Field Programmable Gate Arrays- Programmable Logic Arrays- References- Problems.	9
V	**FLOOR-PLANNING** Introduction - Floor - planning Methods – Block Placement & Channel Definition- Global Routing- switchbox Routing- Power Distribution- Clock Distributions- Floor - planning Tips- Design Validation- Off - Chip Connections – Packages- The I/O Architecture- and PAD Design.	9
	Total Instructional Hours	**45**

Course Outcome

CO1: Design logic gates with minimum size, spacing, and parasitic values.
CO2: Suggest suitable design for logic gates with minimum size, spacing, and parasitic values.
CO3: Design combinational logic machines with optimum power.
CO4: Learn the design principles of FPGA and PLA.
CO5: Suggest various floor planning methods for system design.

TEXT BOOKS:

T1. Wayne Wolf, "Modern VLSI Design – System – on – Chip Design", Prentice Hall, 3rd Edition, 2008.
T2. Michael J. Flynn, Wayne Luk , "Computer System Design: System-on-Chip", Wiley Publications,2003.

REFERENCE BOOKS:

R1. Michel Robert, Bruno Rouzeyre, Christian Piguet, Marie-Lise Flottes, "SOC Design Methodologies", Springer Science & Business Media, 2001.
R2. Steve Furber, "Arm System-On-Chip Architecture", second edition, Pearson Education India, 2002
R3 Peter J. Ashenden, Jean Mermet, Ralf Seepold, "System-on-Chip Methodologies & Design Languages", Springer Science & Business Media, 2002.

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PROGRAMME	COURSE CODE	NAME OF THE COURSE	L	T	P	C
M.E.	16AP3309	WIRELESS ADHOC AND SENSOR NETWORKS	3	0	0	3

Course Objective

1. Develop an understanding of sensor network architectures from design and performance perspective.
2. Learn different types of MAC protocols.
3. Infer basics of adhoc routing protocols.
4. Study the TCP issues in adhoc networks.
5. Learn the architecture and protocols of wireless sensor networks.

Unit	Description	Instructional Hours
I	**INTRODUCTION** Fundamentals of Wireless Communication Technology – The Electromagnetic Spectrum – Radio propagation Mechanisms – Characteristics of the Wireless Channel -mobile ad hoc networks (MANETs) and wireless sensor networks (WSNs): concepts and architectures. Applications of Ad Hoc and Sensor networks. Design Challenges in Ad hoc and Sensor Networks.	9
II	**MAC PROTOCOLS FOR AD HOC WIRELESS NETWORKS** Issues in designing a MAC Protocol- Classification of MAC Protocols- Contention based protocols- Contention based protocols with Reservation Mechanisms- Contention based protocols with Scheduling Mechanisms – Multi channel MAC-IEEE 802.11	9
III	**ROUTING PROTOCOLS AND TRANSPORT LAYER IN AD HOC WIRELESS NETWORKS** Issues in designing a routing and Transport Layer protocol for Ad hoc networks- proactive routing, Reactive routing (on-demand), hybrid routing- Classification of Transport Layer solutions-TCP over Ad hoc wireless Networks.	9
IV	**WIRELESS SENSOR NETWORKS (WSNS) AND MAC PROTOCOLS** Single node architecture: hardware and software components of a sensor node - WSN Network architecture: typical network architectures-data relaying and aggregation strategies -MAC layer Protocols: self-organizing, Hybrid TDMA/FDMA and CSMA based MAC- IEEE 802.15.4.	9
V	**WSN ROUTING, LOCALIZATION & QOS** Issues in WSN routing – OLSR- Localization – Indoor and Sensor Network Localization-absolute and relative localization, triangulation-QOS in WSN-Energy Efficient Design-Synchronization Transport Layer issues.	9
	Total Instructional Hours	**45**

Course Outcome

CO1: Identify different issues in wireless ad hoc and sensor networks.
CO2: Analyze protocols developed for ad hoc and sensor networks.
CO3: Identify and understand security issues in ad hoc and sensor networks.
CO4: Infer the architectures and security issues associated with multicast routing.
CO5: Evaluate the QoS related performance measurements of ad hoc and sensor networks.

TEXT BOOKS:

T1. C.Siva Ram Murthy and B.S.Manoj, "Ad Hoc Wireless Networks – Architectures and Protocols", Pearson Education, 2004.

T2. Carlos De Morais Cordeiro, Dharma Prakash Agrawal, "Ad Hoc and Sensor Networks: Theory and Applications (2nd Edition)", World Scientific Publishing, 2011.

REFERENCE BOOKS:

R1. Holger Karl, Andreas Willig, "Protocols and Architectures for Wireless Sensor Networks", John Wiley & Sons, Inc., 2005.

R2. C.K.Toh, "Ad Hoc Mobile Wireless Networks", Pearson Education, 2009.

R3 Subir Kumar Sarkar, T G Basavaraju, C Puttamadappa, "Ad Hoc Mobile Wireless Networks", Auerbach Publications, 2008.

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PROGRAMME	COURSE CODE	NAME OF THE COURSE	L	T	P	C
M.E.	16AP3310	APPLIED MEDICAL IMAGE PROCESSING	3	0	0	3

Course Objective

1. Learn the fundamentals of medical image processing techniques.
2. Discuss about various medical imaging techniques.
3. Gather knowledge on various forms of representation of medical images.
4. Classify the ways of representing medical images.
5. Infer methods of medical image visualization.

Unit	Description	Instructional Hours
I	**IMAGE FUNDAMENTALS AND PRE-PROCESSING** Image perception- MTF of the visual system- Image fidelity criteria- Image model- Image sampling and quantization – Two dimensional sampling theory- Image quantization- Optimum mean square quantizer- Image transforms – 2D-DFT and other transforms. Image enhancement – point operation- Histogram modeling- spatial operations- Transform operations.	9
II	**BASICS OF MEDICAL IMAGE SOURCES** Radiology- The electromagnetic spectrum-Computed Tomography - Magnetic Resonance Tomography – ultrasound-nuclear medicine and molecular imaging-radiation protection and dosimetry.	9
III	**MEDICAL IMAGE REPRESENTATION** Pixels and voxels – algebraic image operations - gray scale and color representation- depth-colorand look up tables - image file formats- DICOM- other formats- Analyze 7.5 - NifTI and Interfile - Image quality and the signal to noise ratio- MATLAB based simple operations.	9
IV	**MEDICAL IMAGE ANALYSIS AND CLASSIFICATION** Image segmentation- pixel – edge - region based segmentation - Image representation and analysis- Feature extraction and representation- Statistical-Shape- Texture- feature and image classification – Statistical- Rule based- Neural Network approaches.	9
V	**IMAGE REGISTRATIONS AND VISUALIZATION** Rigid body visualization- Principal axis registration- Interactive principal axis registration- Feature based registration- Elastic deformation based registration- Image visualization – 2D display methods- 3D display methods- virtual reality based interactive visualization.	9
	Total Instructional Hours	**45**

Course Outcome

CO1: Compile image processing concepts for medical images.
CO2: Suggest suitable imaging technique for health complications.
CO3: Point out the suitable form of storing the data.
CO4: Elaborate on various analysis of medical images.
CO5: Select suitable method for medical image visualization.

TEXT BOOKS:

T1. Wolfgang Birkfellner, "Applied Medical Image Processing – A Basic course", CRC Press, 2011.
T2. Atam P.Dhawan, "Medical Image Analysis", Wiley Interscience Publication, NJ, USA 2003.

REFERENCE BOOKS:

R1. R.C.Gonzalez and R.E.Woods, "Digital Image Processing", Second Edition, Pearson Education, 2002.
R2. Anil. K. Jain, "Fundamentals of Digital Image Processing", Pearson education, Indian Reprint 2003.
R3 Alfred Horowitz, "MRI Physics for Radiologists – A Visual Approach", Second edition, Springer Verlag Network, 1991.

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