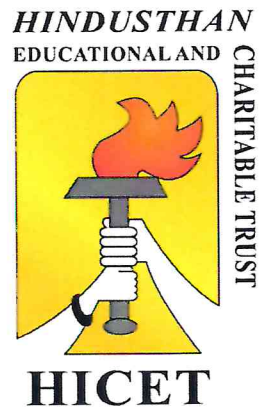


HINDUSTHAN COLLEGE OF ENGINEERING AND TECHNOLOGY
(An Autonomous Institution Affiliated to Anna University, Chennai)
(Approved by AICTE, New Delhi, Accredited by NAAC with 'A' Grade),
COIMBATORE 641 032

M.E. APPLIED ELECTRONICS



Curriculum & Syllabus

2018-2019

VISION AND MISSION OF THE INSTITUTION

VISION

To become a premier institution by producing professionals with strong technical knowledge, innovative research skills and high ethical values.

MISSION


IM1: To provide academic excellence in technical education through novel teaching methods.

IM2: To empower students with creative skills and leadership qualities.

IM3: To produce dedicated professionals with social responsibility.


**Chairman - BoS
EEE - HiCET**




**Dean (Academics)
HiCET**



VISION AND MISSION OF THE DEPARTMENT

VISION

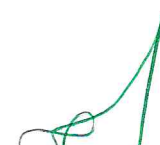
To become a Centre of Excellence in Electrical and Electronics Engineering, in every facet of Engineering Education.

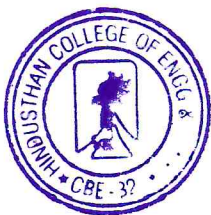
MISSION

- M1. Provide a solid foundation in basic science, mathematics and engineering fundamentals enhancing the student's capability to identify, formulate, analyze and develop solutions for Engineering problems.
- M2. Create an ambiance for the students to develop and flourish their technical skills, design knowledge and innovative ideas to address the environmental issues and sustainable development of the society.
- M3. Inculcate moral values and leadership qualities to meet the challenges of life with courage and confidence.


Chairman - BoS
EEE - HiCET




Dean (Academics)
HiCET



PROGRAM OUTCOMES (POs)

Engineering Graduates will be able to:

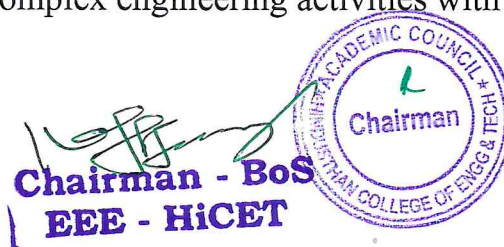
PO 1. **Engineering knowledge:** Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.

PO 2. **Problem analysis:** Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.

PO 3. **Design/development of solutions:** Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.

PO 4. **Conduct investigations of complex problems:** Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.

PO 5. **Modern tool usage:** Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.



Signature of the Dean (Academics) HiCET, with a purple circular stamp that reads 'ACADEMIC COUNCIL - HICET' and 'HINDUSTHAN COLLEGE OF ENGG & TECH.'

PO 6. **The engineer and society:** Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.

PO 7. **Environment and sustainability:** Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.

PO 8. **Ethics:** Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.

PO 9. **Individual and team work:** Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.

PO10. **Communication:** Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.

PO11. **Project management and finance:** Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.

PO12. **Life-long learning:** Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.


**Chairman - BoS
EEE - HiCET**




**Dean (Academics)
HiCET**

PROGRAM SPECIFIC OUTCOMES (PSOs)

- PSO 1. To analyze, design and implement solutions for simple and complex engineering problems that are economically feasible, eco-friendly and socially acceptable solutions in the field of Applied Electronics.
- PSO 2. To apply research and project management skills in Applied Electronics domain concerned with communication system by employing recent technologies.

PROGRAM EDUCATIONAL OBJECTIVES (PEOs)

- PEO 1. To enable graduates to develop solutions to real world problems in the frontier areas of Applied Electronics.
- PEO 2. To enable the graduates to adapt to the latest trends in technology through self-learning and to pursue research to meet out the demands in industries and Academia.
- PEO 3. To enable the graduates to exhibit leadership skills and enhance their abilities through lifelong learning.


Chairman - BoS
EEE - HiCET




Dean (Academics)
HiCET

CURRICULUM

DETAILS OF CHANGES CARRIED OUT IN CURRICULUM & SYLLABUS

CBCS PATTERN

POSTGRADUATE PROGRAMMES

M.E. APPLIED ELECTRONICS
REGULATION 2016

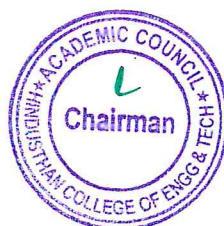
For the students admitted during the academic year 2018-2019 and onwards

SEMESTER I

S.No.	CourseCode	Course Title	L	T	P	C	CIA	ESE	TOTAL
THEORY									
1	16MA1121	Advanced Applied Mathematics	3	1	0	4	40	60	100
2	16AP1201	Embedded Systems	3	0	0	3	40	60	100
3	16AP1202	Advanced Digital Logic System Design	3	1	0	4	40	60	100
4	16AP1203	Advanced Microprocessor and Microcontroller	3	1	0	4	40	60	100
5	16AP13XX	Professional Elective I	3	0	0	3	40	60	100
6	16AP13XX	Professional Elective II	3	0	0	3	40	60	100
PRACTICAL									
7	16AP1001	VLSI Design Laboratory	0	0	4	2	50	50	100
Total Credits:			18	3	4	23	290	410	700

SEMESTER II

S.No.	Course Code	Course Title	L	T	P	C	CIA	ESE	TOTAL
THEORY									
1	16AP2201	Analysis and Design of Analog Integrated Circuits	3	1	0	4	40	60	100
2	16AP2202	ASIC and FPGA Design	3	1	0	4	40	60	100
3	16AP2203	Advanced Digital Signal Processing	3	1	0	4	40	60	100
4	16AP2204	Electromagnetic Interference and Compatibility	3	0	0	3	40	60	100
5	16AP23XX	Professional Elective III	3	0	0	3	40	60	100
6	16AP23XX	Professional Elective IV	3	0	0	3	40	60	100
PRACTICAL									
7	16AP2001	Embedded Systems Laboratory	0	0	4	2	50	50	100
Total Credits:			18	3	4	23	290	410	700



For the students admitted during the academic year 2017-2018 and onwards
SEMESTER III

S.No.	Course Code	Course Title	L	T	P	C	CIA	ESE	TOTAL
THEORY									
1	16AP3201	Computer Architecture and Parallel Processing	3	0	0	3	40	60	100
2	16AP33XX	Professional Elective V	3	0	0	3	40	60	100
3	16AP33XX	Professional Elective VI	3	0	0	3	40	60	100
PRACTICAL									
4	16AP3001	Electronics System Design Laboratory	0	0	4	2	50	50	100
5	16AP3901	Project Phase – I	0	0	12	6	50	50	100
Total Credits:			9	0	16	17	220	280	500

SEMESTER IV

S.No.	Course Code	Course Title	L	T	P	C	CIA	ESE	TOTAL
PRACTICAL									
1	16AP4902	Project Phase - II	0	0	24	12	100	100	200
Total Credits:			0	0	24	12	100	100	200

Total No of Credits: 75

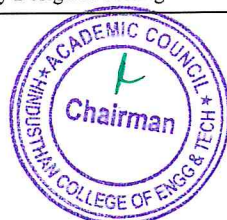
LIST OF PROFESSIONAL ELECTIVES

PROFESSIONAL ELECTIVE I

S.No.	Course Code	Course Title	L	T	P	C	CIA	ESE	TOTAL
THEORY									
1	16AP1301	Advanced Digital Image Processing	3	0	0	3	40	60	100
2	16AP1302	Wireless Mobile Communication	3	0	0	3	40	60	100
3	16AP1303	Intelligent Control and Its Applications	3	0	0	3	40	60	100
4	16AP1304	Digital Control Engineering	3	0	0	3	40	60	100
5	16AP1305	DSP Integrated Circuits	3	0	0	3	40	60	100

PROFESSIONAL ELECTIVE II

S.No.	Course Code	Course Title	L	T	P	C	CIA	ESE	TOTAL
THEORY									
1	16AP1306	CAD for VLSI Circuits	3	0	0	3	40	60	100
2	16AP1307	Multicore Architectures	3	0	0	3	40	60	100
3	16AP1308	Quantum Electronics	3	0	0	3	40	60	100
4	16AP1309	Sensors and Signal Conditioning	3	0	0	3	40	60	100
5	16AP1310	Semiconductor Memory Design & Testing	3	0	0	3	40	60	100



PROFESSIONAL ELECTIVE III

S.No.	CourseCode	Course Title	L	T	P	C	CIA	ESE	TOTAL
THEORY									
1	16AP2301	VLSI Design Techniques	3	0	0	3	40	60	100
2	16AP2302	Embedded Networking	3	0	0	3	40	60	100
3	16AP2303	Fiber Optic Sensors	3	0	0	3	40	60	100
4	16AP2304	Neural Networks and Its Applications	3	0	0	3	40	60	100
5	16AP2305	Medical Imaging Techniques	3	0	0	3	40	60	100

PROFESSIONAL ELECTIVE IV

S.No.	Course Code	Course Title	L	T	P	C	CIA	ESE	TOTAL
THEORY									
1	16AP2306	Low Power VLSI Design	3	0	0	3	40	60	100
2	16AP2307	Research Methodology	3	0	0	3	40	60	100
3	16AP2308	Solid State Device Modeling and Simulation	3	0	0	3	40	60	100
4	16AP2309	High Performance Networks	3	0	0	3	40	60	100
5	16AP2310	Industrial Automation & Control	3	0	0	3	40	60	100

PROFESSIONAL ELECTIVE V

S.No.	Course Code	Course Title	L	T	P	C	CIA	ESE	TOTAL
THEORY									
1	16AP3301	Testing of VLSI Circuits	3	0	0	3	40	60	100
2	16AP3302	Photonics	3	0	0	3	40	60	100
3	16AP3303	Nano Electronics	3	0	0	3	40	60	100
4	16AP3304	Internetworking and Multimedia	3	0	0	3	40	60	100
5	16AP3305	ASIC Design	3	0	0	3	40	60	100

PROFESSIONAL ELECTIVE VI

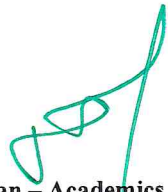
S.No.	Course Code	Course Title	L	T	P	C	CIA	ESE	TOTAL
THEORY									
1	16AP3306	Robotics	3	0	0	3	40	60	100
2	16AP3307	MEMS and NEMS	3	0	0	3	40	60	100
3	16AP3308	System on Chip Design	3	0	0	3	40	60	100
4	16AP3309	Wireless Adhoc and Sensor Networks	3	0	0	3	40	60	100
5	16AP3310	Applied Medical Image Processing	3	0	0	3	40	60	100




CREDIT DISTRIBUTION

Semester	I	II	III	IV	TOTAL
Credits	23	23	17	12	75


Chairman, Board of Studies


Dean – Academics
Dean (Academics)
HiCET


Principal
PRINCIPAL
Hindusthan College Of Engineering & Technology
COIMBATORE - 641 024

SEMESTER I

PROGRAMME	COURSE CODE	NAME OF THE COURSE	L	T	P	C
M.E.	16MA1121	ADVANCED APPLIED MATHEMATICS	3	1	0	4

- Course Objective
1. Apply testing of hypothesis to infer outcome of experiments.
 2. Formulate and construct a mathematical model for a linear programming problem in real life situation.
 3. Understand network modeling for planning and scheduling the project activities.
 4. Develop the ability to use the concepts of Linear Algebra and Special functions for solving problems related to networks.
 5. Acquire knowledge of Fuzzy logic and Fuzzy Algebra.

Unit	Description	Instructional hours
I	TESTING OF HYPOTHESES Sampling distributions -Type I and Type II errors - Tests based on Normal, t, Chi-Square and F distributions for testing of mean, variance and proportions -Tests for Independence of attributes and Goodness of fit.	12
II	LINEAR PROGRAMMING Formulation - Graphical solution - Simplex method - Artificial variable Techniques - Transportation and Assignment Models	12
III	SCHEDULING BY PERT AND CPM Network Construction - Critical Path Method - Project Evaluation and Review technique - Resource Analysis in Network Scheduling.	12
IV	LINEAR ALGEBRA Vector spaces – norms - Inner Products - Eigen values using QR Factorization - generalized eigenvectors - Canonical forms - singular value decomposition and applications -pseudo inverse - least square approximations -Toeplitz matrices and some applications.	12
V	FUZZY LOGIC AND FUZZY ALGEBRA Basic principles of Fuzzy logic - Fuzzy sets of operations - Fuzzy membership Matrix.	12
Total Instructional Hours		60

- Course Outcome
- CO1: Acquire the basic concepts of Statistical techniques for solving mathematical problems which will be useful in solving engineering problems.
- CO2: Apply transportation and assignment models to find optimal solution in warehousing and travelling. Prepare project scheduling using PERT and CPM.
- CO3: Achieve an understanding of the basic concepts of algebraic equations and method of solving them.
- CO4: Analysis the linear algebra QR factorization.
- CO5: Apply the Fuzzy logic in power system problems.

TEXT BOOKS:

- T1. Richard Bronson, Gabriel B.Costa, "Linear Algebra", Academic Press, Second Edition, 2007.
- T2. Richard Johnson., "Miller & Freund's Probability and Statistics for Engineer", Prentice – Hall, Seventh Edition, 2007
- T3. Taha H.A., "Operations Research : An Introduction", 8th Edition, Pearson Education, 2008.

REFERENCE BOOKS:

- R1. Gupta S.C. and Kapoor V.K. "Fundamentals of Mathematical Statistics", Sultan an Sons, 2001.
- R2. Prem Kumar Gupta, D.S. Hira, "Operations Research", S.Chand & Company Ltd, New Delhi, 3rd Edition, 2008.
- R3. Paneer Selvam, 'Operations Research', Prentice Hall of India, 2002.


Chairman - BoS
EEE - HICET




Dean (Academics)
HICET

PROGRAMME	COURSE CODE	NAME OF THE COURSE	L	T	P	C
M.E.	16AP1201	EMBEDDED SYSTEMS	3	0	0	3

- Course Objective
1. Afford awareness about Hardware and software design architecture for embedded Processors with real time examples.
 2. Learn various techniques of embedded system design.
 3. Gain various types of networking and hardware structures.
 4. Study system design for embedded Processor.
 5. Trouble shoot certain modern embedded systems.

Unit	Description	Instructional hours
I	INTRODUCTION Embedded Computers, Characteristics of Embedded Computing Applications, Challenges in Embedded Computing system Design, Embedded system design requirements process, Specification, Architectural Design, Designing Hardware and Software Components, System Integration, Formalism for System Design, Structural Description, Behavioral Description, Design Example: Model Train Controller, ARM processor and memory organization.	9
II	EMBEDDED PROCESSORS SHARC processor Memory organization, Data operations, Flow of Control, parallelism with instructions, CPU Bus configuration, ARM Bus, SHARC Bus, Memory devices, Input/output devices, Component interfacing and debugging, designing with microprocessor development Design Example: Alarm Clock. Hybrid Architecture	9
III	DISTRIBUTED EMBEDDED ARCHITECTURE Hardware and Software Architectures, Networks for embedded systems- I2C, CAN Bus, SHARC link supports, Ethernet, Myrinet, Internet, Network-Based design Communication Analysis, system performance Analysis, Hardware platform design, Allocation and scheduling, Design Example: Elevator Controller.	9
IV	REAL-TIME CHARACTERISTICS Clock driven Approach, weighted round robin Approach, Priority driven Approach, Dynamic Versus Static systems, effective release times and deadlines, Optimality of the Earliest deadline first (EDF) algorithm, challenges in validating timing constraints in priority driven systems, Off-line Versus On-line scheduling.	9
V	SYSTEM DESIGN TECHNIQUES Design Methodologies, Requirement Analysis, Specification, System Analysis and Architecture Design, Quality Assurance, Design Example: Telephone PBX System Architecture, Ink jet printer Hardware Design and Software Design, Personal Digital Assistants, Set-top Boxes.	9
Total instructional hours		45

- Course Outcome
- CO1: Design Hardware and Software architecture for embedded System.
 - CO2: Aware of various techniques of system design.
 - CO3: Design more advanced Embedded based system.
 - CO4: Analyze the programming concepts for embedded systems.
 - CO5: Design the modern embedded systems.

TEXT BOOKS:


- T1. Wayne Wolf, "Computers as Components: Principles of Embedded Computing System Design", Morgan Kaufman Publishers, 2008.
- T2. Jane.W.S. Liu, "Real-Time systems", Pearson Education Asia, 2000.

REFERENCE BOOKS:

- R1. C. M. Krishna and K. G. Shin, "Real-Time Systems", McGraw-Hill, 1997
- R2. Frank Vahid and Tony Givargis, "Embedded System Design: A Unified Hardware / Software Introduction", John Wiley & Sons, 2006.


Chairman - BoS
EEE - HICET




Dean (Academics)
HICET

PROGRAMME	COURSE CODE	NAME OF THE COURSE	L	T	P	C
M.E.	16AP1202	ADVANCED DIGITAL LOGIC SYSTEM DESIGN	3	1	0	4

- Course Objective
1. Basic concepts of Asynchronous Sequential Circuit Design.
 2. Study the concepts of programmable logic devices.
 3. Apply the concepts of System Design Using VHDL and Programmable Devices.
 4. Learn the concepts of fault modeling and fault - tolerant systems.
 5. Gain the concepts of field programmable gate array.

Unit	Description	Instructional hours
I	REVIEW OF DIGITAL SYSTEM DESIGN Designing combinational circuit using multiplexer, decoder – Finite State Machines – Mealy Machine- Moore Machine – State Diagram – State table.	12
II	SYSTEM DESIGN USING PLDS Basic concepts – Programming technologies - Programmable Logic Element (PLE) - Programmable Array Logic (PLA) - Programmable Array Logic (PAL) – Programmable Logic Architectures – 16L8 – 16R4 – 22V10 – Design of combinational and sequential circuits using PLDs – Complex PLDs (CPLDs) –Xilinx cool runner architecture - Design of state machines using Algorithmic State Machines (ASM) chart as a design tool.	12
III	FIELD PROGRAMMABLE GATE ARRAYS Types of FPGA - Xilinx XC3000 series - Logic Cell Array (LCA) – Configurable Logic Blocks (CLB) - Input/Output Blocks (IOB) - Programmable Interconnection Points (PIP) - Xilinx XC4000 Series – FPGA – Design examples.	12
IV	INTRODUCTION TO VHDL Hardware Description Languages – VHDL : Data Objects - Data types - Operators – Entities and Architectures – Concurrent signal assignment – Conditional signal assignment - Selected signal assignment – Concurrent statements – Sequential statements –Delta delays – Behavioral, Data flow and Structural modeling – Attributes – Generics – Packages and Libraries – IEEE 1164 std logic – Subprograms: Functions and Procedures.	12
V	FAULT MODELING AND FAULT - TOLERANT SYSTEMS Defects, errors, faults, Levels of Fault models, Types, Fault Detection in Combinational Logic circuits: Path sensitization method, Boolean difference method. Fault Detection in sequential logic circuit, Design for Testability: Scan path Testing, Boundary Scan Test, Built in Self Test. Fault avoidance and fault - tolerance - Techniques of fault - tolerance - Hardware fault - tolerance: Static and Dynamic	12
Total Instructional Hours		60

- Course Outcome
- CO1: Design and analysis of asynchronous sequential circuit.
CO2: Learn of programmable logic devices.
CO3: Design and carry out of field programmable gate array.
CO4: Explore fault diagnosis and testability algorithm.
CO5: Design and analysis of hardware description languages.

TEXT BOOKS:

- T1. Fundamental of Digital logic design with VHDL-Second edition Stephen Brown/ Zvonko
T2. Digital logic design –Brain Holdsworth and Clive Woods. IV Edition

REFERENCE BOOKS:

- R1. Charles H Roth and Lizy Kurian John “Digital Systems Design Using VHDL,” Cengage Learning,2013.
R2. Bhaskar J., “A VHDL Primer”, Prentice Hall of India learning, 2012.


Chairman - BoS
EEE - HICET




Dean (Academics)
HICET

PROGRAMME	COURSE CODE	NAME OF THE COURSE	L	T	P	C
M.E.	16AP1203	ADVANCED MICROPROCESSOR AND MICROCONTROLLER	3	1	0	4

- Course Objective
1. Gain the architecture and programming of advanced Intel microprocessors and microcontrollers.
 2. Impart the basic knowledge about the Pentium Processors.
 3. Express the basic knowledge about the Arm Processors.
 4. Apply the ARM processors in real time development.
 5. Study about 8 bit microcontrollers PIC.

Unit	Description	Instructional hours
I	MICROPROCESSORS - OVERVIEW Generic Architecture – Instruction Set – Data formats – Addressing modes – Memory hierarchy – Register file – Cache – Virtual memory and paging – Segmentation – Pipelining – The Instruction Pipeline – Pipeline hazards – Instruction level parallelism – Reduced instruction set – Computer principles – RISC versus CISC.	12
II	HIGH PERFORMANCE CISC ARCHITECTURE – PENTIUM CPU Hardware Architecture - Bus Operations – Pipelining – Branch predication – Floating point unit – Operating Modes – Paging – Multitasking – Exception and Interrupts – Instruction set – addressing modes – Programming the Pentium processor (Decimal to Binary and Binary to Decimal).	12
III	HIGH PERFORMANCE RISC ARCHITECTURE – ARM Organization of CPU – Bus architecture – Memory management unit - ARM instruction set – Thumb Instruction set - addressing modes – Programming the ARM processor (Using Thumb Instruction Set).	12
IV	ARM APPLICATION DEVELOPMENT FIR filter – IIR filter – Discrete Fourier transform – Exception handling – Interrupts – Interrupt handling schemes- Firmware and boot loader – Embedded Operating systems – Peripheral Interface – Application of ARM Processor – Caches – Memory protection Units – Memory Management units	12
V	PIC MICROCONTROLLER CPU Architecture – Instruction set – interrupts – Timers – I/O port Expansion - I ² C Interfacing – UART - A/D Converter.	12
Total instructional hours		60

- Course Outcome
- CO1: Learn the fundamentals and architecture of microprocessors.
 - CO2: Illustrate the Pentium architectures and programming.
 - CO3: Describe the ARM architectures and programming.
 - CO4: Develop the ARM processor for real time applications.
 - CO5: Design the basics of PIC microcontroller with programming knowledge.

TEXT BOOKS:

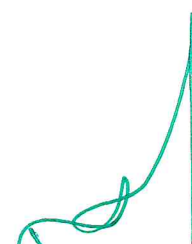
- T1. Daniel Tabak, “Advanced Microprocessors”, McGraw Hill, Inc., 1995.
- T2. James L. Antonakos, “The Pentium Microprocessor” Pearson Education, 1997.

REFERENCE BOOKS:

- R1. Steve Furber, “ARM System – On – Chip architecture”, Addison Wesley, 2000.
- R2. Andrew N. Sloss, Dominic Symes and Chris Wright “ARM System Developer’s Guide : Designing and Optimizing System Software”, First edition, Morgan Kaufmann Publishers, 2004.
- R3. John. B. Peatman, “Design with PIC Microcontroller”, Prentice hall, 1997.


Chairman - BoS
| EEE - HiCET




Dean (Academics)
HiCET

Programme	COURSE CODE	NAME OF THE COURSE	L	T	P	C
M.E.	16AP1001	VLSI DESIGN LABORATORY	0	0	4	2

- Course Objective
1. Learn new software tools for VLSI.
 2. Study various design methods for VLSI circuits.
 3. Gain the knowledge about circuit designing.
 4. Analyze various controllers and its real time Applications.
 5. Propose the Implementation of System using ASIC.

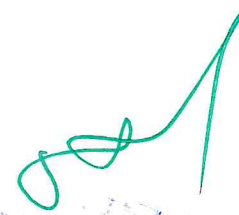
- | Expt. No. | Description of the experiments |
|-----------|---|
| 1. | Design and Simulation of Arithmetic /logic operator circuits using verilog/VHDL |
| 2. | Modeling of Combinational/Sequential Circuits Using Verilog /VHDL |
| 3. | Simulation of schematic /RTL using Xilinx ISE Tool |
| 4. | Design and Implementation of ALU in FPGA using VHDL and Verilog |
| 5. | System design using ASIC |
| 6. | Modeling of Sequential Digital system using Verilog and VHDL |
| 7. | Modeling of MAC unit using verilog / VHDL |
| 8. | Modeling of ALU using verilog / VHDL |
| 9. | Design and 8-bit signed multiplication algorithm using verilog / VHDL |
| 10. | Design and technological mapping of RTL net list in Xilinx ISE Tool |

Total practical hours 45

- Course Outcome
- CO1: Use the software tools for designing and simulation.
CO2: Design the various VLSI circuits using VHDL programming..
CO3: Analyse and design the Implementation of ALU in FPGA using VHDL and Verilog
CO4: Analysis the MAC unit using verilog.
CO5: Design the VLSI circuits using Xilinx ISE tool.


Chairman - BoS
EEE - HICET




Dean (Academics)
HICET

SEMESTER II

PROGRAMME	COURSE CODE	NAME OF THE COURSE	L	T	P	C
M.E.	16AP2201	ANALYSIS AND DESIGN OF ANALOG INTEGRATED CIRCUITS	3	1	0	4

- Course Objective
1. Design the single stage amplifiers using pmos and nmos driver circuits with different loads.
 2. Analyze high frequency concepts of single stage amplifiers and noise characteristics associated with differential amplifiers.
 3. Study the different types of current mirrors and to know the concepts of voltage and current reference circuits.
 4. Gain the various applications in operational amplifier.
 5. Learn the different concepts in stability and frequency compensation.

Unit	Description	Instructional hours
I	SINGLE STAGE AMPLIFIERS Common source stage, Source follower, Common gate stage, Cascade stage, Single ended and differential operation, Basic differential pair, Differential pair with MOS loads	12
II	FREQUENCY RESPONSE AND NOISE ANALYSIS Miller effect, Association of poles with nodes, frequency response of common source stage, Source followers, Common gate stage, Cascade stage, Differential pair, Statistical characteristics of noise, noise in single stage amplifiers, noise in differential amplifiers.	12
III	OPERATIONAL AMPLIFIERS Concept of negative feedback, Effect of loading in feedback networks, operational amplifier performance parameters, One-stage Op Amps, Two-stage Op Amps, Input range limitations, Gain boosting, slew rate, power supply rejection, noise in Op Amps.	12
IV	STABILITY AND FREQUENCY COMPENSATION General considerations, Multipole systems, Phase Margin, Frequency Compensation, and Compensation of two stage Op Amps, Slewing in two stage Op Amps, and Other compensation techniques	12
V	BIASING CIRCUITS Basic current mirrors, cascade current mirrors, active current mirrors, voltage references, supply independent biasing, temperature independent references, PTAT current generation, Constant-Gm Biasing	12
Total instructional hours		60

- Course Outcomes
- CO1: Design and analysis of amplifiers.
 CO2: Acquire of frequency response and noise analysis.
 CO3: Familiarize the Operational Amplifiers.
 CO4: Compose different types of Biasing Circuits.
 CO5: Gain knowledge about the engineering applications of Analog Integrated Circuits.

TEXT BOOKS:

- T1. Paul R. Gray, Paul J. Hurst, Stephen H. Lewis, Robert G. Meyer, Analysis and Design of Analog Integrated Circuits, 5th Edition, Wiley, 2009.
- T2. Behzad Razavi, "Design of Analog CMOS Integrated Circuits", Tata McGraw Hill, 2001.

REFERENCE BOOKS:

- R1. Willey M.C. Sansen, "Analog design essentials", Springer, 2006.
- R2. Grebene, "Bipolar and MOS Analog Integrated circuit design", John Wiley & sons, Inc., 2003.
- R3. Phillip E. Allen, Douglas R. Holberg, "CMOS Analog Circuit Design", Second edition, Oxford University Press, 2002.


Chairman - BoS
EEE - HICET




Dean (Academics)
HICET

PROGRAMME	COURSE CODE	NAME OF THE COURSE	L	T	P	C
M.E.	16AP2202	ASIC AND FPGA DESIGN	3	1	0	4

- Course Objective
1. Learn the design flow of different types of ASIC.
 2. Analyze the synthesis, Simulation and testing of systems.
 3. Familiarize the different types of programming technologies and logic devices.
 4. Know about different high performance algorithms and its applications in ASICs.
 5. Study the logic simulator and Synthesizer

Unit	Description	Instructional hours
I	INTRODUCTION TO ASIC AND LIBRARY DESIGN Types of ASICs - Design flow – Case Study: SPARC Station 1 – Economies of ASICs – ASIC Cell Libraries – CMOS Transistors - Combinational Logic Cell – Sequential logic cell - Data path logic cell – I/O Cells – Transistor Resistance and Parasitic Capacitance - Logical effort – Library cell design - Library architecture.	12
II	PROGRAMMABLE ASIC Anti fuse -Static RAM - EPROM and EEPROM technology – Practical issues - PREP benchmarks - Actel ACT - Xilinx LCA –Altera FLEX - Altera MAX – Xilinx Spartan – Virtex FPGAs – Altera Cyclone FPGAs	12
III	PROGRAMMABLE ASIC I/O DC inputs and Outputs – Totem Pole output –AC inputs and Outputs – Clock input – Power input – Supply bounce – Noise Margin – Meta-stability - Case Study: Xilinx XC4000 IOB	12
IV	PROGRAMMABLE ASIC INTERCONNECT Actel ACT 1/2/3 - Xilinx LCA - Xilinx EPLD - Altera MAX 5000/7000/9000 - Altera FLEX FPGAs – Case study: Spartan-3 Block RAM	12
V	LOGIC SIMULATION & SYNTHESIS Types of simulation – Logic systems – How logic Simulation works – Delay models – Limitations of Logic simulation – Static Timing analysis - Design Systems - Logic synthesis – EDIF – Schematic Entry – Inside a logic Synthesizer – Case Study: Comparator/MUX	12
Total instructional hours		60

- Course Outcome
- CO1: Demonstrate advanced knowledge in programming techniques.
CO2: Apply advanced simulation methods for design circuits.
CO3: Gain knowledge about ASICs and implement in different applications.
CO4: Impart the programming of ASIC Interconnect.
CO5: Compute the programming of ASIC using simulators.

TEXT BOOKS:

- T1. M.J.S .Smith, "Application Specific Integrated Circuits", Addison -Wesley Longman Inc., 2004.
T2. Wayne Wolf, "FPGA-Based System Design", Prentice Hall PTR, 2004.

REFERENCE BOOKS:

- R1. R.Rajsuman and Santa Clara, "System-on-a-Chip Design and Test", CA: Artech House Publishers, 2000.
R2. F.Nekoogar, "Timing Verification of Application-Specific Integrated Circuits (ASICs)", Prentice Hall PTR, 1999.


Chairman - BoS
EEE - HICET




Dean (Academics)
HICET

PROGRAMME	COURSE CODE	NAME OF THE COURSE	L	T	P	C
M.E.	16AP2203	ADVANCED DIGITAL SIGNAL PROCESSING	3	1	0	4

- Course Objective
1. The purpose of this course is to provide indepth treatment on methods in discrete Digital Processing.
 2. Analyze Power spectrum estimation and Random Signal Processing.
 3. Impart knowledge in various types and working of Adaptive Filters.
 4. Apply wavelet transforms.
 5. Analyze the applications of sub band coding.

Unit	Description	Instructional hours
I	DISCRETE RANDOM SIGNAL PROCESSING Random Process - Ensemble Averages - Gaussian Processes-Stationary Process - Auto covariance and auto correlation matrices – Ergodicity – Whitenoise - weiner Khitchine relation- Power spectral density -Spectral Factorization Theorem, Special typeof random process – Signal modeling-Least Squares method, Pade approximation.	12
II	SPECTRUM ESTIMATION Parametric estimation: Bias and consistency Non-Parametric methods –The Periodogram-Correlation method - Co-variance estimator - Performance analysis of various estimators – Unbiased consistent estimators - Periodogram estimator - Barlett spectrum estimation - Welch estimation Model based approach - AR, MA, ARMA Signal modeling -parameter estimation using Yule-Walker method	12
III	LINEAR ESTIMATION AND PREDICTION Maximum likelihood criterion - Efficiency of estimator - Least mean squared error criterion – Wiener filter –Forward and backward prediction, Solution of normal equations - Linear prediction, Prediction error - Whitening filter, Inverse filter - Levinson recursion, Lattice realization, Levinson recursion algorithm for solving Toeplitz system of equations.	12
IV	ADAPTIVE FILTERS Concepts of adaptive filters-FIR Adaptive filters - Newton's steepest descent method - Adaptive filters based on steepest descent method - Widrow Hoff LMS Adaptive algorithm - Adaptive channel equalization - Adaptive echo canceller - Adaptive noise cancellation - RLS Adaptive filters - Exponentially weighted RLS – Sliding window RLS - Simplified IIR LMS Adaptive filter.	12
V	MULTIRATE DIGITAL SIGNAL PROCESSING Mathematical description of change of sampling rate - Interpolation and Decimation - Continuous time model - Direct digital domain approach - Decimation by integer factor - Interpolation by an integer factor - Single and multistage realization - Poly phase realization - Applications to sub band coding - Wavelet transform and filter bank implementation of wavelet expansion of signals.	12
Total instructional hours		60

- Course Outcome
- CO1: Design adaptive filters for a given application.
CO2: Intend analysis of multirate DSP systems.
CO3: Familiarize and Design Adaptive Filters.
CO4: Study and Solve toeplitz equation.
CO5: Apply and Design wavelet transforms in DSP.

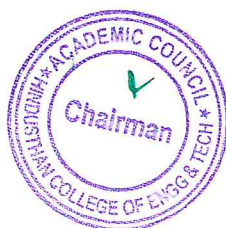
TEXT BOOKS:

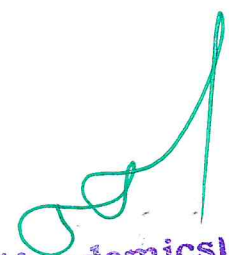
- T1. Monson H. Hayes, "Statistical Digital Signal Processing and Modeling", John Wiley and Sons Inc., New York, 2006.
T2. John G. Proakis, Dimitris G. Manolakis, "Digital Signal Processing", Prentice Hall of India, New Delhi, 2005.

REFERENCE BOOKS:

- R1. Sophoncles J. Orfanidis, "Optimum Signal Processing ", McGraw-Hill, 2000.
R2. Simon Haykin, "Adaptive Filter Theory", Prentice Hall, Englehood Cliffs.


Chairman - BoS
EEE - HICET




Dean (Academics)
HICET

PROGRAMME	COURSE CODE	NAME OF THE COURSE	L	T	P	C
M.E.	16AP2204	ELECTROMAGNETIC INTERFERENCE AND COMPATIBILITY	3	0	0	3

- Course Objective
1. Familiarize with the fundamentals that are essential for electronics industry in the field of EMI/EMC
 2. Provide knowledge on various EMI sources and victims.
 3. Identify the various techniques used in EMC (Electromagnetic compatibility)
 4. Design PCB resistant to EMI
 5. Provide the various international standards in EMI Measurements

Unit	Description	Instructional hours
I	EMI/EMC CONCEPTS EMI-EMC definitions and Units of parameters; Sources and victim of EMI; Conducted and Radiated EMI Emission and Susceptibility; Transient EMI, ESD; Radiation Hazards.	9
II	EMI COUPLING PRINCIPLES Sources of Conducted, and radiated interference; Electromagnetic pulse; possible future interference sources; Interference coupling by Conduction and Radiation. Common ground impedance coupling ; Common mode and ground loop coupling ; Differential mode coupling ; Power mains and Power supply coupling; Design practices employed to minimize interference coupling	9
III	EMI CONTROL TECHNIQUES Shielding, Filtering, Grounding, Bonding, Isolation transformer, Transient suppressors, opto isolators, Cable routing, Signal control	9
IV	PCB DESIGN Transmitter, Receiver, Antenna, Power Supply, Motors, Control devices, Digital Circuits, Digital computer Integrated circuit successability	9
V	EMI MEASUREMENTS AND STANDARDS Open area test site; TEM cell; EMI test shielded chamber and shielded ferrite lined anechoic chamber; Tx /Rx Antennas, Working Principles of EMI sensing Device; EMI Rx and spectrum analyzer; Civilian standards-CISPR, FCC, IEC, EN; Military standards-MIL461E/462.	9
Total instructional hours		45

- Course Outcome
- CO1: Real world EMC design constraints and to achieve the most cost effective design that meets all requirements.
- CO2: Diagnose and solve the basic electromagnetic compatibility problems.
- CO3: Designing the electronic system that function without errors or problems that are related to electromagnetic compatibility.
- CO4: Measuring the EMI with various methods and comparing it with standards.
- CO5: Controlling techniques for EMI and EMC.

TEXT BOOKS:

- T1. V.P.Kodali, "Engineering EMC Principles, Measurements and Technologies", IEEE Press, Newyork, 1996.
- T2. S.Sathyamurthy "Basics of Electromagnetic Compatibility "sams publishers ,2008.

REFERENCE BOOKS:

- R1. Henry W.Ott, "Noise Reduction Techniques in Electronic Systems", A Wiley Inter Science, 1992.
- R2. Bernhard Keiser, "Principles of Electromagnetic Compatibility", 3rd Ed, Artech house, 2008.
- R3. C.R.Paul, "Introduction to Electromagnetic Compatibility", John Wiley and Sons, Inc, 1992.


Chairman - BoS
EEE - HICET




Dean (Academics)
HICET

PROGRAMME	COURSE CODE	NAME OF THE COURSE	L	T	P	C
M.E.	16AP2001	EMBEDDED SYSTEMS LABORATORY	0	0	4	2

- Course Objective
1. Learn and design ARM processor and real time application.
 2. Study and design wireless network using embedded systems.
 3. Design the Implementation of ALU in FPGA using VHDL and Verilog.
 4. Design, simulation and analysis of signal integrity.
 5. Analysis the PIC microcontroller and simulator.

Expt. No.	Description of the experiments
1.	Study of 32 bit ARM7 microcontroller RTOS and its application
2.	Testing RTOS environment and system programming
3.	Designing of wireless network using embedded systems
4.	Implementation of ARM with FPGA
5.	System design using PIC micro controller-Train controller.
6.	Elevator controller using PIC Micro controller
7.	Flash controller programming data flash with erase, verify and fusing
8.	RTC using PIC Micro controller.
9.	Design, simulation and analysis of signal integrity

Total practical hours 45


Chairman - BoS
EEE - HICET




Dean (Academics)
HICET

SYLLABUS

SEMESTER III

PROGRAMME	COURSE CODE	NAME OF THE COURSE	L	T	P	C
M.E.	16AP3201	COMPUTER ARCHITECTURE AND PARALLEL PROCESSING	3	0	0	3

- Course Objective
1. Compare the performance of various computer architectures.
 2. Discriminate between the various data processing architectures.
 3. Infer memory technology and measure its performances.
 4. Describe the performance of various multiprocessor architectures.
 5. Analysis of various multi core architectures.

Unit	Description	Instructional Hours
	COMPUTER DESIGN AND PERFORMANCE MEASURES	
I	Concepts of Computer Design – Parallel and Scalable Architectures –Multiprocessors –Multivector and SIMD architectures - Multi threaded architectures – Data-flow architectures - Performance Measures.	9
	PARALLEL PROCESSING, PIPELINING AND ILP	
II	Instruction Level Parallelism and Its Exploitation - Concepts and Challenges –Overcoming Data Hazard with Dynamic Scheduling Dynamic Branch Prediction - Speculation - Multiple Issue Processors - Performance and Efficiency in Advanced Multiple Issue Processors.	9
	MEMORY HIERARCHY DESIGN	
III	Memory Hierarchy - Memory Technology and Optimizations – Cache memory – Optimizations of Cache Performance –Memory Protection and Virtual Memory -Design of Memory Hierarchies.	9
	MULTIPROCESSOR	
IV	Symmetric and distributed shared memory architectures –Cache coherence issues – Performance Issues – Synchronization issues – Models of Memory Consistency -Interconnection networks – Buses, crossbar and multistage switches.	9
	MULTI-CORE ARCHITECTURES	
V	Software and hardware multithreading – SMT and CMP architectures – Design issues –Case studies – Intel Multi-core architecture ARM processor Multicore architecture – BUS protocol for Multicore architecture.	9
Total Instructional Hours		45

- Course outcome
- CO1: Categorize the performance of various architectures.
 CO2: Prioritize the best performing architectures.
 CO3: Design memories under various hierarchies.
 CO4: Estimate the performance of various multiprocessor architectures.
 CO5: Choose the suitable multi core architecture based on the applications.

TEXT BOOKS:

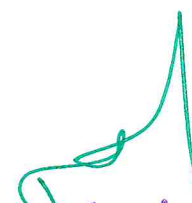
- T1. Kai Hwang, "Advanced Computer Architecture", McGraw Hill International, 2001.
 T2. John L. Hennessy and David A. Patterson, "Computer Architecture – A quantitative approach", Morgan Kaufmann / Elsevier, 4th Edition, 2007.

REFERENCE BOOKS:

- R1. David E. Culler, Jaswinder Pal Singh, "Parallel Computing Architecture: A hardware/ software Approach", Morgan Kaufmann / Elsevier, 1997.
 R2. John P. Shen, "Modern processor design. Fundamentals of super scalar processors", Tata McGraw Hill 2003.
 R3. William Stallings, "Computer Organization and Architecture Designing for Performance", Pearson Education, Seventh Edition, 2006.


Chairman - BoS
EEE - HICET




Dean (Academics)
HICET

PROGRAMME	COURSE CODE	NAME OF THE COURSE	L	T	P	C
M.E.	16AP3901	PROJECT PHASE - I	0	0	12	6

- Course Objective
1. Analyze a methodology to select a project and able to develop a hardware/software project.
 2. Transform the ideas behind the project with clarity.
 3. Validate the technical report.

Description of the project work

A candidate is permitted to work on projects in an Industrial / Research Organization, on the recommendations of the Head of the Department concerned.

A project must be selected either from research literature published list or the students themselves may propose suitable topics in consultation with their guide.

The aim of the project work is to strengthen the comprehension of principles by applying them to a new problem which may be the design and manufacture of a device, a research investigation or a design problem.

The project work shall be supervised by a supervisor of the department, (and an expert in industry if it is a industrial project), and the student shall be instructed to meet the supervisor periodically and to attend the review committee meeting for evaluation of the progress.

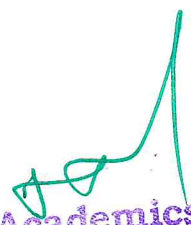
In case of candidates not completing Phase-I of project work successfully, the candidates can undertake Phase-I again in the subsequent semester. In such cases the candidates can enroll for Phase-II, only after successful completion of Phase-I.

The Project report shall be prepared and submitted according to the approved guidelines as given by the Controller of Examination and bonafied duly signed by Supervisor and the Head of the Department.

- Course Outcome
- CO1: Realize the skills acquired in the previous semesters to solve complex engineering problems.
 - CO2: Build up an innovative model / prototype of an idea related to the field of specialization.
 - CO3: Create the work individually to identify, troubleshoot and build products for environmental and societal issues.
 - CO4: Effective presentation of ideas with clarity.
 - CO5: Evaluate surveys towards developing a product which helps in life time learning.


Chairman - BoS
EEE - HICET




Dean (Academics)
HICET

SEMESTER IV

PROGRAMME	COURSE CODE	NAME OF THE COURSE	L	T	P	C
M.E.	16AP4902	PROJECT PHASE - II	0	0	24	12

Course Objective	1. Analyze a methodology to select a project and able to develop a hardware/software project.
	2. Transform the ideas behind the project with clarity.
	3. Validate the technical report.

Description of the project work

The Project work (Phase II) shall be pursued for a minimum prescribed period as per regulation.

The project work shall be supervised by a supervisor of the department, (and an expert in industry if it is a industrial project), and the student shall be instructed to meet the supervisor periodically and to attend the review committee meeting for evaluation of the progress.

The Project report shall be prepared and submitted according to the approved guidelines as given by the Controller of Examination and bonafied duly signed by Supervisor and the Head of the Department.

Course Outcome	CO1: Realize the skills acquired in the previous semesters to solve complex engineering problems.
	CO2: Build up an innovative model / prototype of an idea related to the field of specialization.
	CO3: Create the work individually to identify, troubleshoot and build products for environmental and societal issues.
	CO4: Effective presentation of ideas with clarity.
	CO5: Evaluate surveys towards developing a product which helps in life time learning.


Chairman - BoS
EEE - HICET




Dean (Academics)
HICET

PROFESSIONAL ELECTIVE 1

PROGRAMME	COURSE CODE	NAME OF THE COURSE	L	T	P	C
M.E.	16AP1301	ADVANCED DIGITAL IMAGE PROCESSING	3	0	0	3

- Course Objective
1. Learn the image fundamentals and mathematical transforms necessary for image processing . Study the image enhancement techniques.
 2. Revise the image segmentation and representation techniques.
 3. Independently design and carry out the basic knowledge in image Compression
 4. Study the basic knowledge about Image Filtering And Restoration

Unit	Description	Instructional hours
I	DIGITAL IMAGE FUNDAMENTALS Elements of digital image processing system-Image sensing and acquisition- Image sampling and quantization – Basic relationship between Pixels	9
II	IMAGE TRANSFORMS AND IMAGE ENHANCEMENT Need for image transforms- Discrete Wavelet transform- Harr Wavelets- Spatial domain methods- Frequency domain methods- Histogram modification techniques-median filtering- Low pass filtering- averaging of multiple images- - high pass filtering.	9
III	IMAGE FILTERING AND RESTORATION Image observation models- restoration in the presence of noise only- spatial filtering: mean filters, order statistics filters, adaptive filters- Inverse filtering- Wiener filtering – Constrained least squares filtering- blind deconvolution.	9
IV	IMAGE SEGMENTATION AND REPRESENTATION Edge detection: Gradient operators-edge linking and boundary detection: Global processing via Hough transform, Graph theoretic techniques-Thresholding: Global thresholding, adaptive threshold-Representation: Chain codes, Polygonal approximations, Signatures, boundary segments, skeletons-Boundary descriptors: Shape numbers, Fourier descriptors, Statistical moments-Regional descriptors: Texture-Relational descriptors.	9
V	IMAGE COMPRESSION JPEG-MPEG-Quantization: scalar Quantization and vector Quantization-code word assignment: uniform length and variable length codeword assignment – differential pulse code modulation, two channel coders, pyramid coding; hybrid transform coding – wavelet coding.	9
Total instructional hours		45


- Course Outcome
- CO1: Apply image processing techniques in both the spatial and frequency (Fourier) domains.
 CO2: Design image analysis techniques in the form of image segmentation and to evaluate the methodologies for segmentation.
 CO3: Independently design and carry out the image Filtering .
 CO4: Describe the image enhancement techniques.
 CO5: Discuss the Restoration and Compression.

TEXT BOOKS:

- T1. Gonzalez R.C. Woods R.E, "Digital Image Processing", Prentice Hall; 2007
 T2. Jain A.K., "Fundamentals of Digital Image Processing", Prentice Hall of India,1989

REFERENCE BOOKS:

- R1. Kenneth R Castleman, "Digital Image Processing", Prentice Hall International, Inc., 2001.
 R2. William K.Pratt,"Digital Image Processing", John Wiley & Sons, 2007.


Chairman - BoS
EEE - HICET




Dean (Academics)
HICET

PROGRAMME	COURSE CODE	NAME OF THE COURSE	L	T	P	C
M.E.	16AP1302	WIRELESS MOBILE COMMUNICATION	3	0	0	3

- Course Objective
1. Analyze the wireless channel and its physical design.
 2. Understand the concepts of digital modulation.
 3. Recognize concepts in selection of channel.
 4. Comprehend the concepts of various spread spectrum.
 5. Learn the multiuser systems.

Unit	Description	Instructional hours
I	THE WIRELESS CHANNEL Overview of wireless systems – Physical modeling for wireless channels – Time and Frequency coherence – Statistical channel models – Capacity of wireless Channel- Capacity of Flat Fading Channel , Channel Distribution Information known – Channel Side Information at Receiver – Channel Side Information at Transmitter and Receiver – Capacity with Receiver diversity	9
II	PERFORMANCE OF DIGITAL MODULATION OVER WIRELESS CHANNEL Fading– Outage Probability– Average Probability of Error – Combined Outage and Average Error Probability – Doppler Spread – Inter symbol Interference	9
III	DIVERSITY Realization of Independent Fading Paths – Receiver Diversity – Selection Combining– Threshold Combining – Maximal-Ratio Combining – Equal - Gain Combining – Transmitter Diversity – Channel known at Transmitter – Channel unknown at Transmitter– The Alamouti Scheme.	9
IV	MULTICARRIER MODULATION Data Transmission using Multiple Carriers – Multicarrier Modulation with Overlapping Sub channels – Mitigation of Subcarrier Fading – Discrete Implementation of Multicarrier Modulation – Peak to average Power Ratio- Frequency and Timing offset – Case study IEEE 802.11a.	9
V	SPREAD SPECTRUM Spread Spectrum Principles – Direct Sequence Spread Spectrum – Spreading Codes Synchronization- RAKE receivers- Frequency Hopping Spread Spectrum – Multiuser DSSS Systems – Multiuser FHSS Systems	9
Total instructional hours		45

- Course Outcome
- CO1: Demonstrate advanced knowledge in wireless networks
CO2: Analyze and understand the digital communication and modulation
CO3: Apply appropriate techniques and tools to complex engineering activities in the field of wireless networks.
CO4: Design and analyse the multicarrier modulation.
CO5: Impart the knowledge on the multiuser systems.

TEXT BOOKS:

- T1. Andrea Goldsmith, Wireless Communications, Cambridge University Press, 2005.
T2. David Tse and Pramod Viswanath, Fundamentals of Wireless Communication, Cambridge University Press, 2005.

REFERENCE BOOKS:

- R1. W.C.Y.Lee, Mobile Communication Engineering, Mc Graw Hill, 2000.
R2. A.Paulraj, R.Nabar, D.Gore, Introduction to Space-Time Wireless Communication, Cambridge University Press, 2003.


Chairman - BoS
EEE - HICET




Dean (Academics)
HICET

PROGRAMME	COURSE CODE	NAME OF THE COURSE	L	T	P	C
M.E.	16AP1303	INTELLIGENT CONTROL AND ITS APPLICATIONS	3	0	0	3

Course Objective

1. Study the basic concepts about Soft computing.
2. Impart the knowledge of Genetic Algorithm and Intelligent control.
3. Acquire knowledge about Neural Networks and Fuzzy Logic systems.
4. Provide knowledge on hybrid soft computing techniques..
5. Discuss about the various applications of soft computing techniques in engineering.

Unit	Description	Instructional hours
I INTRODUCTION	Evolution of computing-Soft Computing constituents and conventional Artificial Intelligence-Learning methods-taxonomy-Evolution of neural networks-basic models-Important Technologies-Weights,Bias, Threshold, Learning rate- Introduction to Neuro – Fuzzy and Soft Computing – Fuzzy Sets – Basic Definition and Terminology – Set-theoretic Operations. Genetic algorithm- Introduction Biological background-traditional optimization and search techniques	9
II GENETIC ALGORITHM	Genetic Algorithm and search space-general genetic algorithm-operators-General Cycle – Stopping condition-constraints-Building block hypothesis, working principle, basic operators and technologies-Genetic modeling: Significance of Genetic operators, inheritance operator, inversion & deletion, Bitwise operator.GA optimization problems- Job Shop Scheduling Problem(JSPP)	9
III NEURAL NETWORKS	Machine Learning using Neural work, Adaptive Network-Feed Forward Networks-Supervised Learning Neural Networks – Perceptrons - Adaline – Back propagation Multilayer Perceptrons – Unsupervised Learning Neural Networks – Competitive Learning Networks – Kohonen Self-Organizing Networks – Learning Vector Quantization	9
IV FUZZY LOGIC	Membership functions: features, fuzzification, methods of membership value assignments- Defuzzification: lambda cuts – methods – fuzzy arithmetic and fuzzy measures: fuzzy arithmetic – extension principle – fuzzy measures – measures of fuzziness -fuzzy integrals – fuzzy rule base and approximate reasoning : truth values and tables, fuzzy reasoning-fuzzy inference systems-overview of fuzzy expert system-fuzzy decision making.	9
V HYBRID SOFT COMPUTING TECHNIQUES & APPLICATIONS	Neuro-fuzzy hybrid systems – genetic Neuro hybrid systems – genetic fuzzy hybrid and fuzzy genetic hybrid systems – simplified fuzzy ARTMAP – Applications: A fusion approach of multispectral images with SAR, optimization of traveling salesman problem (TSP) using genetic algorithm approach -Real-Time adaptive control of a Direct Drive Motor-GA Fuzzy systems for control of flexible Robots.	9
Total instructional hours		45

- Course Outcome**
- CO1: Observe the basic concept about soft computing.
 - CO2: Carry out about Intelligent control and its applications.
 - CO3: Explain about Neural Networks and Fuzzy Logic operations.
 - CO4: Acknowledge the function of Hybrid soft computing Techniques.
 - CO5: Apply the various applications of soft computing techniques in engineering.

TEXT BOOKS:

- T1. J.S.R.Jang, C.T. Sun and E.Mizutani, “Neuro-Fuzzy and Soft Computing”, PHI / Pearson Education 2012
- T2. S.N.Sivanandam and S.N.Deepa, “Principles of Soft Computing”, Wiley India Pvt Ltd, 2011

REFERENCE BOOKS:

- R1. L.Fortuna,G.Rizzotto,M.Lavorgna,G,Nunnari,M.G.Xibilia and R.Caponetto, “Soft Computing New Trends and Applications”,Springer 2011.
- R2. Fakhreddine O. Karray Clarence De Silva, “Soft Computing and Intelligent Systems-Design,Theory,Tools and Applications”,Pearson Education 2009


Chairman - BoS
EEE - HiCET




Dean (Academics)
HiCET

PROGRAMME	COURSE CODE	NAME OF THE COURSE	L	T	P	C
M.E.	16AP1304	DIGITAL CONTROL ENGINEERING	3	0	0	3

- Course Objective
1. Study the basics of digital control systems and sampling.
 2. Introduce the z-domain in digital control system.
 3. Familiarize state variable analysis of digital control systems.
 4. Analyze the stability of discrete time systems.
 5. Understand the various design techniques on digital control system.

Unit	Description	Instructional hours
I	INTRODUCTION Overview of frequency and time response analysis and specifications of control systems - Digital control systems – basic concepts of sampled data control systems – principle of sampling, quantization and coding – Reconstruction of signals – Sample and Hold circuits – Practical aspects of choice of sampling rate -Basic discrete time signals – Time domain models for discrete time systems.	9
II	MODELS OF DIGITAL CONTROL DEVICES AND SYSTEMS Z domain description of sampled continuous time plants – models of A/D and D/A converters – Z Domain description of systems with dead time – Implementation of digital controllers – Digital PID controllers – Position, velocity algorithms – Tuning – Zeigler – Nichols tuning method.	9
III	STATE VARIABLE ANALYSIS OF DIGITAL CONTROL SYSTEMS State space representation of discrete time systems – Solution of discrete time state space equation – State transition matrix – Decomposition techniques – Controllability and Observability – Multivariable discrete systems.	9
IV	STABILITY ANALYSIS Mapping between S plane and Z plane- Jury's stability test - Routh stability criterion- Liapunov Stability Analysis of discrete time systems	9
V	DESIGN OF DIGITAL CONTROL SYSTEM Z plane specifications of control system design – Digital compensator design – Frequency response method - State feedback – Pole placement design – State Observers – Digital filter properties – Frequency response – Kalman's filter.	9
Total instructional hours		45

- Course Outcome
- CO1: Use the basic knowledge of sampling in digital control systems.
CO2: Develop the different models and digital controllers of control systems.
CO3: Pertain the different techniques to digital control systems by the concepts of State variable analysis.
CO4: Apply the techniques to observe the stability of the control systems.
CO5: Design the digital control system.

TEXT BOOKS:

- T1. Gopal M. "Digital Control and State Variable methods", Tata McGraw Hill Publishing Company Ltd., New Delhi, India, 2003.
T2. M. Sami Fadali. "Digital Control Engineering Analysis and Design", Elsevier Inc, 2013.

REFERENCE BOOKS:

- R1. M.Gopal. "Digital Control Engineering", New age International (p) Ltd, 1999.
R2. Ogata K. "Discrete Time Control Systems", Prentice Hall International", New jersey, USA, 2002.


Chairman - BoS
EEE - HICET




Dean (Academics)
HICET

PROGRAMME	COURSE CODE	NAME OF THE COURSE	L	T	P	C
M.E.	16AP1305	DSP INTEGRATED CIRCUITS	3	0	0	3

- Course Objective
1. Learn how DSP applications are implemented using VLSI Technology.
 2. Compare and study the performance of various transforms for signal processing.
 3. Design FIR and IIR filters for the given specifications.
 4. Impart the knowledge about DSP Processor Architecture using VLSI Technology.
 5. Design Integrated circuits using VLSI Technology.

Unit	Description	Instructional hours
I	DSP INTEGRATED CIRCUITS AND VLSI CIRCUIT TECHNOLOGIES Standard digital signal processors, Application specific IC's for DSP, DSP systems, DSP system design, Integrated circuit design. MOS transistors, MOS logic, VLSI process technologies, Trends in CMOS technologies.	9
II	DIGITAL SIGNAL PROCESSING Digital signal processing, Sampling of analog signals, Selection of sample frequency, Signal-processing systems, Frequency response, Transfer functions, Signal flow graphs, Filter structures, Adaptive DSP algorithms, DFT-The Discrete Fourier Transform, FFT-The Fast Fourier Transform Algorithm, Image coding, Discrete cosine transforms.	9
III	DIGITAL FILTERS AND FINITE WORD LENGTH EFFECTS FIR filters, FIR filter structures, FIR chips, IIR filters, Specifications of IIR filters, Mapping of analog transfer functions, Mapping of analog filter structures, Multirate systems, Interpolation with an integer factor L, Sampling rate change with a ratio L/M, Multirate filters. Finite word length effects –Parasitic oscillations, Scaling of signal levels, Round-off noise, Measuring round-off noise, Coefficient sensitivity, Sensitivity and noise.	9
IV	DSP ARCHITECTURES AND SYNTHESIS OF DSP ARCHITECTURES DSP system architectures, Standard DSP architecture, Ideal DSP architectures, Multiprocessors and multicomputers, Systolic and Wave front arrays, Shared memory architectures. Mapping of DSP algorithms onto hardware, Implementation based on complex PEs, Shared memory architecture with Bit – serial PEs.	9
V	ARITHMETIC UNITS AND INTEGRATED CIRCUIT DESIGN Conventional number system, Redundant Number system, Residue Number System, Bit-parallel and Bit- Serial arithmetic, Basic shift accumulator, Reducing the memory size, Complex multipliers, Improved shift-accumulator. Layout of VLSI circuits, FFT processor, DCT processor and Interpolator as case studies.	9
Total instructional hours		45

- Course Outcome
- CO1: Solve discrete-time transforms.
CO2: Design FIR and IIR filters.
CO3: Knowledge of spectral estimation and linear prediction.
CO4: Apply above knowledge and skills to engineering problems.
CO5: Design Integrated Circuits using VLSI Technology.

TEXT BOOKS:

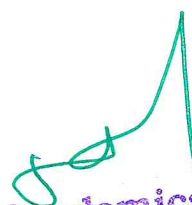
- T1. Lars Wanhammer, "DSP Integrated Circuits", 1999 Academic press, New York
T2. A.V.Oppenheim et.al, "Discrete-time Signal Processing", Pearson Education, 2000.

REFERENCE BOOKS:

- R1. Emmanuel C. Ifeachor, Barrie W. Jervis, "Digital signal processing – A practical approach" Second Edition, Pearson Education, Asia.
R2. Keshab K.Parhi, "VLSI Digital Signal Processing Systems design and Implementation", John Wiley & Sons, 1999.


Chairman - BoS
EEE - HICET




Dean (Academics)
HICET

PROFESSIONAL ELECTIVE II

PROGRAMME	COURSE CODE	NAME OF THE COURSE	L	T	P	C
M.E.	16AP1306	CAD FOR VLSI CIRCUITS	3	0	0	3

- Course Objective
1. Analyze various physical design methods in VLSI.
 2. Comprehend the concepts behind the VLSI design rules and routing techniques.
 3. Use the simulation techniques at various levels in VLSI design flow.
 4. Understand the concepts of various algorithms used for floor planning and routing techniques.
 5. Study of high level transformation.

Unit	Description	Instructional hours
I	BASIC OF CAD ALGORITHMS Introduction to VLSI Design methodologies - Review of Data structures and algorithms – Review of VLSI Design automation tools - Algorithmic Graph Theory and Computational Complexity – Tractable and Intractable problems - General purpose methods for combinatorial optimization .	9
II	LAYOUT DESIGN ALGORITHMS Layout Compaction - Design rules - Problem formulation - Algorithms for constraint graph compaction -Placement and partitioning - Circuit representation - Placement algorithms – Partitioning.	9
III	P&R ALGORITHMS Floor planning concepts - Shape functions and floorplan sizing - Types of local routing problems -Area routing - Channel routing - Global routing - Algorithms for global routing.	9
IV	SIMULATION AND SYNTHESIS ALGORITHMS Simulation - Gate-level modeling and simulation - Switch-level modeling and simulation - Combinational Logic Synthesis - Binary Decision Diagrams - Two Level Logic Synthesis.	9
V	SYSTEM MODELING ALGORITHMS High level Synthesis - Hardware models - Internal representation - Allocation - Assignment and scheduling - Simple scheduling algorithm - Assignment problem – High level transformations.	9
Total instructional hours		45

- Course Outcome
- CO1: Demonstrate advanced knowledge in design techniques.
 CO2: Analyze and understand the design algorithms.
 CO3: Apply advanced simulation methods for design circuits.
 CO4: Understand the concepts of various algorithms used for floor planning and routing techniques.
 CO5: Study of high level transformation.

TEXT BOOKS:

- T1. S.H. Gerez, "Algorithms for VLSI Design Automation", John Wiley & Sons, 2 Edition, 2006.
 T2. N.A. Sherwani, "Algorithms for VLSI Physical Design Automation", Kluwar Academic Publishers, 2002.

REFERENCE BOOKS:

- R1. Drechsler,R., Evolutionary Algorithms for VLSI CAD, Kluwer Academic Publishers, Boston, 1998.
 R2. Eugene D.Fabricius, "Introduction to VLSI Design", McGraw Hill International Editions, 1990.


**Chairman - BoS
 EEE - HICET**




**Dean (Academics)
 HICET**

PROGRAMME	COURSE CODE	NAME OF THE COURSE	L	T	P	C
M.E.	16AP1307	MULTICORE ARCHITECTURES	3	0	0	3

- Course Objective
1. Appreciate the need for parallel processing.
 2. Understand the recent trends in the field of Computer Architecture and identify performance related parameters.
 3. Expose the students to the problems related to multiprocessing.
 4. Understand the different types of multicore architectures.
 5. Expose the students to warehouse-scale and embedded architectures.

Unit	Description	Instructional hours
I	FUNDAMENTALS OF QUANTITATIVE DESIGN AND ANALYSIS Classes of Computers – Trends in Technology, Power, Energy and Cost – Dependability – Measuring, Reporting and Summarizing Performance – Quantitative Principles of Computer Design – Classes of Parallelism - ILP, DLP, TLP and RLP - Multithreading - SMT and CMP Architectures – Limitations of Single Core Processors - The Multicore era.	9
II	DLP IN VECTOR, SIMD AND GPU ARCHITECTURES Introduction- Vector Architecture - SIMD Instruction Set Extensions for Multimedia – Graphics Processing Units - Detecting and Enhancing Loop Level Parallelism.	9
III	TLP AND MULTIPROCESSORS Introduction- Centralized shared memory Architectures- Symmetric and Distributed Shared Memory Architectures – Cache Coherence Issues - Performance Issues – Synchronization Issues – Models of Memory Consistency – Interconnection Networks – Buses, Crossbar and Multi-stage Interconnection Networks.	9
IV	RLP AND DLP IN WAREHOUSE-SCALE ARCHITECTURES Introduction- Programming Models and Workloads for Warehouse-Scale Computers – Architectures for Warehouse-Scale Computing – Physical Infrastructure and Costs – Cloud Computing.	9
V	ARCHITECTURES FOR EMBEDDED SYSTEMS Features and Requirements of Embedded Systems – Signal Processing and Embedded Applications – The Digital Signal Processor – Embedded Multiprocessors	9
Total instructional hours		45

- Course Outcome
- CO1: Identify the limitations of ILP and the need for multicore architectures.
CO2: Discuss the issues related to multiprocessing and suggest solutions.
CO3: Point out the salient features of different multicore architectures and how they exploit Parallelism.
CO4: Develop the knowledge of embedded system.
CO5: Analyse the embedded based architectures.

TEXT BOOKS:

- T1. John L. Hennessey and David A. Patterson, “Computer Architecture – A Quantitative Approach”, Morgan Kaufmann / Elsevier, 5th edition, 2012.

REFERENCE BOOKS:

- R1. Kai Hwang, “Advanced Computer Architecture”, Tata McGraw-Hill Education, 2003.
R2. Richard Y. Kain, “Advanced Computer Architecture a Systems Design Approach”, Prentice Hall, 2011.



[Handwritten Signature]
Chairman - BoS
EEE - HICET

[Handwritten Signature]
Dean (Academics)
HICET

PROGRAMME	COURSE CODE	NAME OF THE COURSE	L	T	P	C
M.E.	16AP1308	QUANTUM ELECTRONICS	3	0	0	3

- Course Objective
1. Know the concepts of EM fields and wave equation
 2. Study the types of lasers and its characteristics
 3. Learn the concept of Non-linear optics
 4. Identify the various methods of scattering
 5. Gain knowledge of the concept of noise in amplifiers and oscillators

Unit	Description	Instructional hours
I	BASIC THEOREMS AND FACTS OF QUANTUM MECHANICS Introduction to Quantum Electronics-History of quantum electronics-Recent progress in quantum electronics-Planar-mirror waveguides-Modes in dielectric slab waveguides-Effective Index Method-Guided wave coupling and Interference-Coupled Mode Theory-Directional coupler-Mode coupling in periodic waveguides-Mode Interference-The Schrodinger wave equation-Matrix formulation of quantum mechanics-Lattice vibration and their quantization, Electromagnetic fields and their quantization.	9
II	LASER Gaussian beam in a homogenous medium, lens waveguide, Elliptic Gaussian beams, Optical resonators, Spontaneous and induced transitions, gain coefficient, homogenous and inhomogeneous broadening, Laser oscillations, Semiconductor laser, quantum well laser, modulation of optical radiation, Q switching and Mode locking of laser, Quantum wires and dots, Laser arrays-Laser Oscillation-specific laser systems-semiconductor diode lasers-Quantum well lasers- Free electron laser.	9
III	NON LINEAR OPTICS Introduction to non linear optics -The nonlinear optical susceptibility tensor, Electromagnetic Formulation of the Nonlinear Interaction-Optical Second harmonic generation, parametric amplification, parametric oscillations – conservation laws-Birefringence and Quasi- Phase Matching-3 rd order NL effects-Self-Phase Modulation, Optical soliton-Electro-optic (EO) modulation of light-Linear EO effect, Phase retardation-Amplitude, and Phase modulation-Traveling wave modulator	9
IV	STIMULATED RAMAN AND BRILLOUIN SCATTERING Introduction-Stimulated Molecular Raman scattering, Electromagnetic treatment of Stimulated Raman Scattering - Anti stokes scattering, Stimulated Brillouin scattering, self focusing of optical beams.	9
V	NOISE AND SPECTRA OF LASER AMPLIFIERS AND OSCILLATORS Noise in laser amplifiers-Spontaneous Emission Noise in Laser Oscillators - Laser spectra - laser spectra Experiments – The α Parameter - Measurement of $(\Delta\nu)_{laser}$.	9
Total instructional hours		45

- Course Outcome
- CO1: Appreciate the importance of wave guides.
CO2: Realize the importance of laser.
CO3: Gain knowledge about non linear optics and its types.
CO4: Understand the concepts of scattering.
CO5: Identify the noise in amplifiers and oscillators.

TEXT BOOKS:

- T1. Amnon Yariv, "Quantum Electronics", John Wiley 1989.
T2. Max Schubert, Bernd Wilhelmi, "Nonlinear optics and quantum electronics", Wiley-Interscience 1986.

REFERENCE BOOKS:

- R1. D.Marcuse, "Principle of Quantum Electronics", Cambridge 1980.
R2. Max Schubert, Bernd Wilhelmi, "Nonlinear optics and quantum electronics", Wiley-Interscience 1986.


Chairman - BoS
EEE - HICET




Dean (Academics)
HICET

PROGRAMME	COURSE CODE	NAME OF THE COURSE	L	T	P	C
M.E.	16AP1309	SENSORS AND SIGNAL CONDITIONING	3	0	0	3

- Course Objective
1. Identify the static and dynamic characteristics of measurement systems.
 2. Acquire knowledge about various types of sensors viz. Resistive, Reactive, Self- generating.
 3. Analyse various signal conditioning circuits.
 4. Impart knowledge about different types digital sensors.
 5. Illustrate semiconductor sensors and special sensors.

Unit	Description	Instructional hours
I	INTRODUCTION TO MEASUREMENT SYSTEMS Introduction to measurement systems: general concepts and terminology, measurement systems, sensor classification, errors, static characteristics of measurement systems, accuracy, precision, sensitivity, linearity, resolution, dynamic characteristics of zero-order, first-order, and second-order measurement systems.	9
II	RESISTIVE SENSORS Resistive sensors: potentiometer, strain gauges and types, resistive temperature detector(RTD), thermistor, light-dependent resistors(LDR); Signal conditioning for resistive sensors: measurement of resistance , voltage dividers, Wheatstone bridge, sensor bridge calibration and compensation, differential amplifier, instrumentation amplifier.	9
III	REACTIVE SENSORS Reactance variation and electromagnetic sensors: capacitive sensors, inductive sensors – reluctance variation, eddy current, linear variable differential transformers (LVDTs), electromagnetic sensors – sensors based on faraday’s law, hall effect sensor; Signal conditioning for capacitive sensors, carrier amplifiers – application to the LVDT.	9
IV	SELF-GENERATING SENSORS Self-generating sensors: thermoelectric sensors, piezoelectric sensors, pyroelectric sensors, photovoltaic sensors, electrochemical sensors, Signal conditioning for self-generating sensors: chopper amplifiers, electrometer amplifiers, charge amplifiers.	9
V	DIGITAL SENSORS AND SEMICONDUCTOR DEVICE SENSORS Digital sensors: position encoders, resonant sensors –vibrating wire strain gauges, digital flow meters, thermometers based on semiconductor junctions, photodiodes and phototransistors, charge-coupled sensors – types of CCD imaging sensors, ultrasonic-based sensors, fiber-optic sensors.	9
Total instructional hours		45

- Course Outcome
- CO1: Analyse the static and dynamic characteristics of measurement systems.
CO2: Acquire knowledge about the various types of sensors viz. Resistive, Reactive, Self-generating and their signal conditioning.
CO3: Examine various signal conditioning circuits.
CO4: Impart knowledge about different types digital sensors.
CO5: Illustrate semiconductor sensors and special sensors.

TEXT BOOKS:

- T1. Ramon Pallás Areny, John G. Webster, “Sensors and Signal Conditioning”, 2nd edition, John Wiley and Sons, 2000.
T2. D.Patranabis, “Sensors and Transducers”, Tata McGraw Hill Publications, 2003.

REFERENCE BOOKS:

- R1. E.O. Doebelin, “Measurement System : Applications and Design”, McGraw Hill Publications.
R2. C.D. Johnson, “Process Control Instrumentation Technology”, John Wiley and Sons.


Chairman - BoS
EEE - HICET




Dean (Academics)
HICET

PROGRAMME	COURSE CODE	NAME OF THE COURSE	L	T	P	C
M.E.	16AP1310	SEMICONDUCTOR MEMORY DESIGN AND TESTING	3	0	0	3

- Course Objective
1. Study the architectures for SRAM, DRAM and various non-volatile memories.
 2. Study the fault modeling and testing of memories for fault detection.
 3. Learn the radiation hardening process and issues for memory.
 4. Discuss the recent memory technologies.
 5. Study about memory package.


Unit	Description	Instructional hours
I	RANDOM ACCESS MEMORY TECHNOLOGIES Static Random Access Memories (SRAMs): SRAM Cell Structures-MOS SRAM Architecture-MOS SRAM Cell and Peripheral Circuit Operation-Bipolar SRAM Technologies-Silicon On Insulator (SOI) Technology-Advanced SRAM Architectures and Technologies-Application Specific SRAMs. Dynamic Random Access Memories (DRAMs): DRAM Technology Development-CMOS DRAMs DRAMs Cell Theory and Advanced Cell Structures-BiCMOS, DRAMs-Soft Error Failures in DRAMs-Advanced DRAM Designs and Architecture-Application, Specific DRAMs.	9
II	NON VOLATILE MEMORIES Masked Read-Only Memories (ROMs)-High Density ROMs-Programmable Read-Only Memories (PROMs)-BipolarPROMs-CMOS PROMs-Erasable (UV) - Programmable Read-Only Memories (EPROMs)-Floating-Gate EPROM Cell-One-Time Programmable (OTP) EPROMs-Electrically Erasable PROMs (EEPROMs)-EEPROM Technology And Architecture-Nonvolatile SRAM-Flash Memories (EPROMs or EEPROM)-Advanced Flash Memory Architecture.	9
III	MEMORY FAULT MODELING, TESTING AND FAULT TOLERANCE RAM Fault Modeling, Electrical Testing, Pseudo Random Testing-Megabit DRAM Testing Nonvolatile Memory Modeling and Testing-IDDQ Fault Modeling and Testing-Application Specific Memory Testing.	9
IV	RELIABILITY AND RADIATION EFFECTS General Reliability Issues - RAM Failure Modes and Mechanism-Nonvolatile Memory Reliability-Reliability Modeling and Failure Rate Prediction-Design for Reliability Test Structures-Reliability Screening and Qualification. Radiation Effects-Single Event Phenomenon (SEP) - Radiation Hardening Techniques Radiation Hardening Process and Design Issues-Radiation Hardened Memory Characteristics-Radiation Hardness Assurance and Testing - Radiation Dosimetry-Water Level Radiation Testing and Test Structures.	9
V	ADVANCED MEMORY TECHNOLOGIES AND PACKAGING TECHNOLOGIES Ferroelectric Random Access Memories (FRAMs)-Gallium Arsenide (GaAs) FRAMs-Analog Memories-Magneto resistive Random Access Memories-Random Access Memories (MRAMs)-Experimental Memory Devices. Memory Hybrids and MCMs (2D)-Memory Stacks and MCMs (3D)-Memory MCM Testing and Reliability Issues-Memory Cards High Density Memory Packaging Future Directions.	9
	Total instructional hours	45
Course Outcome	CO1: Study the architectures for SRAM, DRAM and non-volatile memories. CO2: Learn the knowledge about the fault modeling and testing of memories for fault detection. CO3: Acquire knowledge about radiation hardening process and issues for memory. CO4: Impart the concepts of advanced memory technologies and packing technologies. CO5: Familiarize the memory technology and packaging technologies.	

TEXT BOOKS:

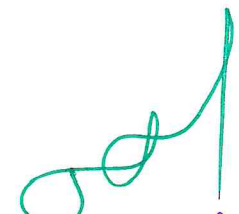
- T1. Ashok K.Sharma, " Semiconductor Memories Technology, Testing and Reliability ",Prentice Hall of India Private Limited, New Delhi, 1997.

REFERENCE BOOKS:

- R1. Luecke Mize Care, "Semiconductor Memory design & application", Mc-Graw Hill.
R2. Betty Prince, "Emerging Memories: Technologies and Trends", Kluwer Academic publishers, 2002


Chairman - BoS
EEE - HICET




Dean (Academics)
HICET

PROFESSIONAL ELECTIVE III

PROGRAMME	COURSE CODE	NAME OF THE COURSE	L	T	P	C
M.E.	16AP2301	VLSI DESIGN TECHNIQUES	3	0	0	3

- Course Objective
1. Study the basic of MOS Circuits
 2. Design and carry out the MOS Process Technology.
 3. Learn the VLSI fabrication and lay out designing the operation of MOS devices
 4. Impart in-depth knowledge about analog and digital CMOS circuits.
 5. The depth knowledge about the logic design

Unit	Description	Instructional hours
I	OVERVIEW OF VLSI DESIGN METHODOLOGY VLSI design process - Architectural design - Logical design – Physical design - Layout styles - Full custom - Semicustom approaches.	9
II	BASIC ELECTRICAL PROPERTIES OF MOS AND CMOS CIRCUITS MOS transistor - Threshold voltage equations -Basic DC equations - Second order effects - MOS models - Small signal AC characteristics - NMOS inverter - Depletion mode and enhancement mode pull ups – CMOS inverter - DC characteristics - Inverter delay - Pass transistor - Transmission gate –Power consumption in CMOS gates – Static dissipation – Dynamic Dissipation.	9
III	VLSI FABRICATION TECHNIQUES AND LAYOUT DESIGN RULES An overview of wafer fabrication – Wafer processing - Oxidation - Patterning – Diffusion - Ion implantation - Deposition – Silicon gate NMOS process - CMOS processes - NWell - PWell - Twintub - Silicon on insulator - CMOS process enhancements - Interconnect - Circuit elements- Latch up - Latchup prevention techniques. Need for design rules - Mead Conway design rules for the silicon gate NMOS process – CMOS based design rules	9
IV	LOGIC DESIGN Switch logic - Pass transistor and transmission gate based design - Gate logic - Inverter - Two input NAND gate - NOR gate - Other forms of CMOS logic – Dynamic CMOS logic - Clocked CMOS logic - Precharged domino CMOS logic - Structured design - Simple combinational logic design examples - Parity generator - Multiplexers – Clocked sequential circuits - Two phase clocking - Charge storage - Dynamic register element - NMOS and CMOS - Dynamic shift register -Semistatic register - JK flip flop circuit.	9
V	SUBSYSTEM DESIGN PROCESS General arrangement of a 4-bit arithmetic processor - Design of a 4bit shifter - Design of a ALU subsystem - Implementing ALU functions with an adder - Carry look ahead adders - Multipliers - Serial parallel multipliers – Pipelined multiplier array – Modified Booth's algorithm - Incrementer / Decrementer.	9
Total instructional hours		45


- Course Outcome
- CO1: Analysis the operation of CMOS
 CO2: Study of the design rules and layout diagram.
 CO3: Design of basic electrical properties of mos and cmos circuits
 CO4: Impart in-depth knowledge about analog and digital CMOS circuits.
 CO5: Apply and implementing of the logic design.

TEXT BOOKS:

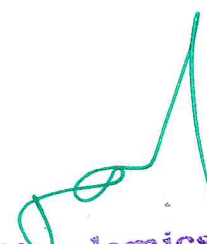
- T1. Kamran Eshraghian, Douglas A. Pucknell, *Essentials of VLSI Circuits and Systems*, Prentice Hall of India, 2011
 T2. Neil Weste and Kamran Eshranghian, *Principles of CMOS VLSI Design*, Addison Wiley, 2012.

REFERENCE BOOKS:

- R1. Jan M Rabaey, *Digital Integrated Circuits- A Design*, Prentice Hall, 2009
 R2. S.Srinivasan, *VLSI Circuits*, NPTEL Courseware, 2005.


Chairman - BoS
EEE - HICET




Dean (Academics)
HICET

PROGRAMME	COURSE CODE	NAME OF THE COURSE	L	T	P	C
M.E.	16AP2302	EMBEDDED NETWORKING	3	0	0	3

- Course Objective
1. Impart knowledge on Serial and parallel communication protocols
 2. Application Development using USB and CAN bus for PIC microcontrollers
 3. Application development using Embedded Ethernet
 4. Basic knowledge about elements of a network
 5. Development using Wireless sensor network communication protocols

Unit	Description	Instructional hours
I	COMMUNICATION PROTOCOLS Serial/Parallel Communication – Serial communication protocols -RS232 standard – RS485 – Synchronous Serial Protocols -Serial Peripheral Interface (SPI) – Inter Integrated Circuits (I2C) – PC Parallel port programming - ISA/PCI Bus protocols – Firewire.	9
II	USB AND CAN BUS USB bus – Introduction – Speed Identification on the bus – USB States – USB bus communication: Packets –Data flow types –Enumeration –Descriptors –PIC Microcontroller USB Interface – CAN Bus – Introduction - Frames –Bit stuffing –Types of errors –Nominal Bit Timing – PIC microcontroller CAN Interface –A simple application with CAN.	9
III	ETHERNET BASICS Elements of a network – Inside Ethernet – Building a Network: Hardware options – Cables, Connections and network speed – Design choices: Selecting components – Ethernet Controllers – Using the internet in local and internet communications.	9
IV	EMBEDDED ETHERNET Exchanging messages using UDP and TCP – Serving web pages with Dynamic Data – Serving web pages that respond to user Input – Email for Embedded Systems – Using FTP – Keeping Devices and Network secure.	9
V	WIRELESS EMBEDDED NETWORKING Wireless sensor networks – Introduction – Applications – Network Topology – Localization –Time Synchronization - Energy efficient MAC protocols –SMAC – Energy efficient and robust routing – Data Centric routing.	9
Total instructional hours		45

- Course Outcome
- CO1: Complete knowledge of wired and wireless network protocols.
CO2: Should be able to incorporate networks in embedded systems.
CO3: Apply the TCP,IP,ISA client server protocols for embedded networks.
CO4: Design and carry out the basic knowledge about elements of a network.
CO5: Independently design and carry out Wireless sensor network communication protocols.

TEXT BOOKS:

- T1. Frank Vahid, Tony Givargis, “Embedded Systems Design: A Unified Hardware/Software Introduction” - John & Wiley Publications, 2002.
- T2. Jan Axelson, “Parallel Port Complete: Programming, interfacing and using the PCs parallel printer port” - Penram Publications, 1999

REFERENCE BOOKS:

- R1. Dogan Ibrahim, “Advanced PIC microcontroller projects in C: from USB to RTOS with the PIC18F series” - Elsevier 2008.
- R2. Jan Axelson, “Embedded Ethernet and Internet Complete”, Penram publications, 2003.


Chairman - BoS
| EEE - HiCET




Dean (Academics)
HiCET

PROGRAMME	COURSE CODE	NAME OF THE COURSE	L	T	P	C
M.E.	16AP2303	FIBER OPTIC SENSORS	3	0	0	3

- Course Objective
1. Illustrate the fundamentals of Fiber Optic Sensor Technology.
 2. Explore the fiber Grating Sensors.
 3. Discuss the types of distributed and magnetic sensors.
 4. Compare the use of Chemical and Bio sensors.
 5. Generalize the applications of fiber optic sensors.

Unit	Description	Instructional hours
I	SENSOR TECHNOLOGY The Emergence of Fiber Optic Sensor Technology -Introduction to Optical Fibers-Types of optical Fibers , Step-Index single mode and multimode Fiber - Intensity-Based and Interferometric Sensors - Fabry perot, Mach Zender, Michelson and Sagnac.	9
II	GRATING SENSORS Multimode Grating and Polarisation Sensors-Sensors Based on Relative Movement of Opposed Gratings-Grating Period Modulation-Sensors Based on the Photoelastic Effect- Retardation Plates-Fiber Grating Sensors.	9
III	DISTRIBUTED AND MAGNETIC SENSORS Fiber Optic Distributed and Magnetic Sensor-Distributed Sensing- Basic Principles of Sensor Multiplexing- Interferometric Sensor Multiplexing- Faraday effect sensors-Magneto strictive - Lorentz force sensors-Evanescence Field Absorption Sensors	9
IV	CHEMICAL AND BIOSENSOR Fiber Optic Chemical and Biosensor: Reagent Mediated sensor-Humidity sensor – pH sensor - Hydrogen sensor - CO ₂ sensor – Ammonia sensor - Chloride sensor – Glucose sensor – Oxygen sensor - Surface Plasmonic Resonance based sensor.	9
V	APPLICATIONS Industrial Applications of Fiber Optic Sensors : Temperature – Pressure - Fluid level – flow – Position - Vibration - Rotation measurements - Current - Voltage measurement – Chemical analysis	9
Total instructional hours		45

- Course Outcome
- CO1: Apply the important of fiber optics technology
 - CO2: Analyze the fiber Grating Sensors
 - CO3: Illustrate the types of distributed and magnetic sensors
 - CO4: Differentiate the working of Chemical and Bio sensor
 - CO5: Categorize the applications of fiber optic sensors.

TEXT BOOKS:

- T1. Eric Udd, William B. Spillman, Jr., "Fiber Optic Sensors: An Introduction for Engineers and Scientists", John Wiley & Sons 2011.
- T2. Francis T.S. Yu, Shizhuo Yin, Paul B. Ruffin, "Fiber Optic Sensors", CRC Press Publisher 2010.

REFERENCE BOOKS:

- R1. Bhagavānadāsa Gupta, Bansi Das Gupta, "Fiber Optic Sensors: Principles and Applications", New India Publishing 2006.
- R2. David A. Krohn, "Fiber optic sensors: fundamentals and applications", ISA Publishing 2000.


Chairman - BoS
EEE - HICET




Dean (Academics)
HICET

PROGRAMME	COURSE CODE	NAME OF THE COURSE	L	T	P	C
M.E.	16AP2304	NEURAL NETWORKS AND ITS APPLICATIONS	3	0	0	3

- Course Objective
1. Introduce the basic knowledge about neural networks.
 2. Impart knowledge on various learning processes and propagation techniques.
 3. Survey attractive applications of artificial neural networks.
 4. Study the self organization maps.
 5. Analyze various applications of neuro dynamics.

Unit	Description	Instructional hours
I	INTRODUCTION What is neural network? Human brain - models of a neuron – neural network viewed as directed graph – network architectures- knowledge representation- artificial intelligence and neural networks- error correction learning.	9
II	LEARNING PROCESS AND SINGLE LAYER PERCEPTION Competitive-Boltzmann learning-credit assignment problem-Memory-adaption-adaptive filtering problem-unconstrained organization techniques-least mean square algorithm-convergence theorem-relation between perception and bayes classifier for a Gaussian environment -engineering applications.	9
III	BACK PROPAGATION Back propagation algorithm XOR problem-heuristics-output representation and decision rule-back propagation and differentiation-hessian matrix - generalization-cross validation-network pruning techniques-virtues and limitations of back propagation learning-back propagation network applications.	9
IV	SELF ORGANISATION MAPS Two basic feature mapping models-self organization map-SOM algorithm-properties of feature map-computer simulations-learning vector quantization- adaptive patter classification-hierarchical vector quantizer - contextmel maps –applications of self organizing maps.	9
V	NEURO DYNAMICS Dynamical system- stability of equilibrium states-attractors-neuro dynamical models-manipulation of attractors' as a recurrent network paradigm –Hopfield models-Hopfield networks applied to travelling salesman problem	9
Total instructional hours		45

- Course Outcome
- CO1: Apply the basic knowledge of neural networks on engineering applications
 - CO2: Recall various learning processes in neural networks and its applications.
 - CO3: Analyze self organization maps and their applications.
 - CO4: Apply neural networks in real time applications.
 - CO5: Pertain various applications of neuro dynamics

TEXT BOOKS:

- T1. Simon Haykin , “ Neural Networks - A Comprehensive foundation ”, Pearson education, second edition,2004.
- T2. James A. Freeman, David M.Skapura, “Neural Network Algorithm, Applications and Programming Techniques”, Pearson education,2007.

REFERENCE BOOKS:

- R1. Huajin Tang, Kay chen Tan, Zhang Yi, “Neural Networks: Computational Models and Applications”, Springer, 2010.
- R2. James A. Anderson , “ An Introduction to Neural Networks”, prentice-hall of India pvt.ltd.2002.
- R3. S.N. Sivanandam, S.Sumathi, S.N.Deepa, “Introduction to Fuzzy Logic using MATLAB”, Springer,2003


Chairman - BoS
| EEE - HICET




Dean (Academics)
HICET

PROGRAMME	COURSE CODE	NAME OF THE COURSE	L	T	P	C
M.E.	16AP2305	MEDICAL IMAGING TECHNIQUES	3	0	0	3

- Course Objective
1. Discuss need for quality control and quality control test in X ray.
 2. Study the functioning of radioisotopic imaging equipments.
 3. Know about MRI, image acquisition and reconstruction and MRI safety.
 4. Gain the mathematical concept needed in image processing.
 5. Understand about medical image processing techniques.

Unit	Description	Instructional hours
I	PRINCIPLES OF RADIOGRAPHIC EQUIPMENT X-Ray tubes, cooling systems, removal of scatters, Fluoroscopy-construction of image Intensifier tubes, angiographic setup, mammography, digital radiology, DSA.	9
II	COMPUTED TOMOGRAPHY Need for sectional images, Principles of sectional scanning, CT detectors, Methods of reconstruction, Iterative, Back projection, convolution and Back Projection. Artifacts, Principle of 3D imaging	9
III	RADIO ISOTOPIC IMAGING Alpha, Beta and Gamma radiation, Radiation detectors, Radio isotopic imaging equipments, Radio nuclides for imaging, Gamma ray camera, scanners, Positron Emission tomography, SPECT,PET/CT	9
IV	ULTRASONIC SYSTEMS Wave propagation and interaction in Biological tissues, Acoustic radiation fields, continuous and pulsed excitation, Transducers and imaging systems, Scanning methods, Imaging Modes, Principles and theory of image generation	9
V	MAGNETIC RESONANCE IMAGING NMR, Principles of MRI, Relaxation processes and their measurements, Pulse sequencing and MR image acquisition, MRI Instrumentation, Functional MRI	9
Total instructional hours		45

- Course Outcome
- CO1: Domain knowledge about the various Medical Imaging techniques.
CO2: Explain the various diagnostic applications of the medical imaging techniques.
CO3: Acquired the knowledge about the functioning of radio isotopic imaging equipments, MRI, image acquisition and reconstruction and MRI safety.
CO4: Understand the mathematical and medical concept needed in image processing.
CO5: Analyse the ultrasonic systems.

TEXT BOOKS:

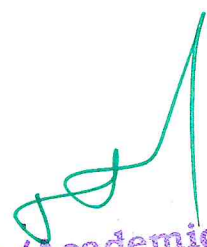
- T1. D.N.Chesney and M.O.Chesney Radio graphic imaging, CBS Publications, New Delhi, 1987.
T2. Peggy, W., Roger D.Ferimarch, MRI for Technologists, Mc Graw Hill, New York, 1995.

REFERENCE BOOKS:

- R1. Steve Webb, The Physics of Medical Imaging, Taylor & Francis, New York.1988
R2. Donald W.McRobbice, Elizabeth A.Moore, Martin J.Grave and Martin R.Prince MRI from picture to proton ,Cambridge University press, New York 2006.
R3. Jerry L.Prince and Jnathan M.Links, Medical Imaging Signals and Systemsl-Pearson Education Inc. 2006


Chairman - BoS
EEE - HICET




Dean (Academics)
HICET

PROFESSIONAL ELECTIVE IV

PROGRAMME	COURSE CODE	NAME OF THE COURSE	L	T	P	C
M.E.	16AP2306	LOW POWER VLSI DESIGN	3	0	0	3

- Course Objective
1. Identify the various power losses in an IC.
 2. Categorize the power reduction techniques based on optimization.
 3. Employ suitable techniques to reduce the power losses.
 4. Design memory circuits with less power losses.
 5. Use software in VLSI design.

Unit	Description	Instructional hours
I	LOW POWER CMOS VLSI DESIGN Basic principles and limits of low power VLSI design– Sources of Power dissipation – Physics of Power dissipation in CMOS FET devices – Power Dissipation in CMOS – Short Circuit, Dynamic, Load Capacitance	9
II	POWER OPTIMIZATION Pre Computation Based Optimization - Logic Level Power Optimization – FSM and Combinational Logic Synthesis – Technology Mapping – Circuit Level Optimization – Circuit Level Transforms – CMOS Gate – Transistor Sizing.	9
III	DESIGN AND TEST OF LOW VOLTAGE CMOS CIRCUITS Circuit Design Style- Leakage current in deep sub micrometer transistors- Deep sub micrometer device design issue- low voltage circuit design techniques-Testing deep sub micrometer ICs with elevated intrinsic leakage.	9
IV	POWER ESTIMATION Power Estimation Techniques –Probabilistic –Statistical – Power Sensitivity Estimation –Estimation Glitching Power –Power Estimation Using Input Vector Compaction – Genetic Algorithm Maximum Power Estimation Strategies Power Saving in Interconnect.	9
V	SYNTHESIS AND SOFTWARE DESIGN FOR LOW POWER Behavioral level transforms - Sources of Power dissipation – Software power Estimation – Software power optimization – Automated Low power Code Generation – Co-design for low power.	9
Total instructional hours		45

- Course Outcome
- CO1: Discuss the various sources of power losses in Integrated Circuits.
 CO2: Enumerate the different power reduction techniques.
 CO3: Select Suitable techniques and adopt them to reduce the power loss.
 CO3: Design and Estimate power in VLSI circuits.
 CO5: Design given VLSI circuits using Softwares.

TEXT BOOKS:

- T1. Kaushik Roy and S.C.Prasad, “Low power CMOS VLSI circuit design”, Wiley, 2000. Kluwer, 2002.
- T2. Dimitrios Soudris, Chirstian Pignet, Costas Goutis, “Designing CMOS Kluwer, 2002

REFERENCE BOOKS:

- R1. J.B.Kulo and J.H.Lou, “Low voltage CMOS VLSI Circuits”, Wiley 1999.
- R2. A.P.Chandrasekaran and R.W.Broadersen, “Low power digital CMOS design”, Kluwer, 1995
- R3. Chirstian Pignet “Low Power CMOS Circuits” CRC Press, Taylor & Francis Group, 2010.



[Signature]
Chairman - BoS
EEE - HiCET

[Signature]
Dean (Academics)
HiCET

PROGRAMME	COURSE CODE	NAME OF THE COURSE	L	T	P	C
M.E.	16AP2307	RESEARCH METHODOLOGY	3	0	0	3

- Course Objective
1. Impart scientific knowledge for carrying out research work effectively.
 2. Study about the various Research Design.
 3. Acquire knowledge about Experimental design and Data collection
 4. Provide knowledge in multivariate analysis techniques
 5. Discuss about the Research Practices and Report writing.

Unit	Description	Instructional hours
I	INTRODUCTION TO RESEARCH Research-Definition-Objectives of research, Meaning of research- Characteristics of research -Importance of research activities- Types of research-Research approaches-Significance-Problems in research- Qualities of good researcher- Research process-Problem encountered by researchers in India.	9
II	RESEARCH DESIGN The nature of research designs-Formulation of the research design: Process-classification of research designs-Exploratory-Secondary resource analysis-Two-tired research design- Concepts used in experiments-Validity in experimentation-factors affecting external validity-classification of experimental design-Pre-experimental-Quasi-experimental designs.	9
III	DATA COLLECTION METHODS Classification of Data-Collection of primary data-Observation-Interview method-Collection of data through Questionnaires-schedules-collection of secondary data-Research applications of secondary data-Benefits and drawbacks-classification of secondary data-Internal –External data sources-Presentation of data.	9
IV	MULTIVARIATE ANALYSIS TECHNIQUES Growth of Multivariate techniques-Characteristics and applications-Classification-Variables in multivariate analysis-Important multivariate techniques-Factor analysis-Rotation in factor analysis-R-type and Q type factor analysis-Path analysis.	9
V	RESEARCH PRACTICE AND REPORT WRITING. Literature review-Conference proceedings-Journals-Journal Impact Factor(JFI)-Citation index-h-index-Significance of report writing-Different steps in writing report-Layout of report writing-Types of reports-Mechanics of writing a research report-precautions for writing research reports-Conclusion and Scope for future work-Oral presentation.	9
Total instructional hours		45

- Course Outcome
- CO1: Observe the various approaches to do research.
CO2: Carryout the research design.
CO3: Acknowledge the function of Multivariate Analysis Techniques.
CO4: Carryout the data collection for research activities.
CO5: Organize the research activity systematically and prepare research report effectively.

TEXT BOOKS:

- T1. C.R.Kothari, Research Methodology Methods & Techniques, NEW Age International (P) Limited, New Delhi, 2007.
- T2. Dr.Deepak Chawla, Dr. Neena Sondhi, Research Methodology concepts and cases,Vikas Publishing House Pvt. Ltd.New Delhi, 2011

REFERENCE BOOKS:

- R1. K.Prathapan, Research Methodology for Scientific Research, I.K.International Publishing House Pvt.Ltd. New Delhi, 2014L.
- R2. R.Panneerselvam, Research Methodology, PHI Learning Private Limited, New Delhi, 2011.
- R3. Donald H.McBurney, Research Methods, Thomson Asia Pvt. Ltd. Singapore, 2002.


Chairman - BoS
EEE - HICET




Dean (Academics)
HICET

PROGRAMME	COURSE CODE	NAME OF THE COURSE	L	T	P	C
M.E.	16AP2308	SOLID STATE DEVICE MODELING AND SIMULATION	3	0	0	3

- Course Objective
1. Observe the fundamentals of circuit design and device modeling.
 2. Study principles of device modeling where in device physics and expressions for device Performance under various scenarios of excitation.
 3. Apply the design and modeling of Noise Modeling
 4. Impart the knowledge of BSIM mosfet modeling.
 5. Discuss the most widely used device models used by the industry including BSIM and EKV models.

Unit	Description	Instructional hours
I	MOSFET DEVICE PHYSICS MOSFET capacitor, Basic operation, Basic modeling, Advanced MOSFET modeling, RF modeling of MOS transistors, Equivalent circuit representation of MOS transistor, High frequency behavior of MOS transistor and A.C small signal modeling, model parameter extraction, modeling parasitic BJT, Resistors , Capacitors, Inductors.	9
II	MOSFET MODELING Basic modeling, SPICE Level - 1, 2 and 3 models, Short channel effects, Advanced MOSFET modeling, RF modeling of MOS transistors, Equivalent circuit representation of MOS transistor, High frequency behavior of MOS transistor and A.C small signal modeling.	9
III	NOISE MODELING Noise sources in MOSFET, Flicker noise modeling, Thermal noise modeling, model for accurate distortion analysis, nonlinearities in CMOS devices and modeling, calculation of distortion in analog CMOS circuit.	9
IV	BSIM4 MOSFET MODELING Gate dielectric model, Enhanced mode 1 for effective DC and AC channel length and width, Threshold voltage model, Channel charge model, Mobility model, source/drain resistance model, I - V model, gate tunneling current model, substrate current models, Capacitance models, High speed model, RF model, Noise model, Junction diode models, Layout - dependent parasitic model.	9
V	OTHER MOSFET MODELS The EKV model, model features, long channel drain current model, modeling second order effects of the drain current, modeling of charge storage effects, Non - quasi static modeling, Noise model, temperature effects, MOS model 9, MOSAI model, PSP model, Influence of process variation, Modeling of device mismatch for Analog/RF Applications.	9
Total instructional hours		45

- Course Outcome
- CO1: Gain the basic circuit design and device modeling for analysis.
CO2: Acquire principles of device modeling and device performance under various scenarios of excitation.
CO3: Design the high speed model of MOSFET.
CO4: Adequate the most widely used device models used by the industry including BSIM and EKV models.
CO5: Study the EKV models of MOS semiconductors.

TEXT BOOKS:

- T1. Trond Ytterdal, Yuhua Cheng and Tor A. Fjeldly, Wayne Wolf, "Device Modeling for Analog and RF CMOS Circuit Design", John Wiley & Sons Ltd.
- T2. Selberherr, S., "Analysis and Simulation of Semiconductor Devices", Springer - Verlag. , 1984.

REFERENCE BOOKS:

- R1. Arora, N., "MOSFET Models for VLSI Circuit Simulation", Springer - Verlag, 1993.
- R2. B.G.Streetman and S. Banarjee, "Solid State Electronic Devices", Prentice - Hall of India Pvt. Ltd, New Delhi, India.
- R3. B. Bhattacharyya, "Compact MOSFET Models for VLSI Design", John Wiley & Sons Inc., 2009.



[Signature]
Chairman - BoS
EEE - HICET

[Signature]
Dean (Academics)
HICET

PROGRAMME	COURSE CODE	NAME OF THE COURSE	L	T	P	C
M.E.	16AP2309	HIGH PERFORMANCE NETWORKS	3	0	0	3

- Course Objective
1. Develop a comprehensive understanding of multimedia networking.
 2. Study the types of VPN and tunneling protocols for security.
 3. Learn about network security in many layers and network management.
 4. Study the concept of SMI, MIB & SNMP.
 5. Impart the knowledge on network security and management.

Unit	Description	Instructional hours
I	NETWORKING BASICS Evolution of networks – network models – network elements – mods of communication – review of network models, Switching, Routing. Broad band technologies: SONET – DWDM – DSL – ISDN – BISDN, ATM.	9
II	MULTIMEDIA NETWORKING APPLICATIONS Streaming stored and live Audio and Video – Best effort service and its limitations – real interactive audio and video, protocols– audio and video compression – beyond best effort service – scheduling and policing mechanism – integrated services –RSVP-differentiated services.	9
III	ADVANCED NETWORKS CONCEPTS VPN-Remote-Access VPN, site-to-site VPN, Tunneling to PPP, Security in VPN.MPLS- operation, Routing, Tunneling and use of FEC, Traffic Engineering, MPLS based VPN, overlay networks-P2P connections, USB Tethering, IPv6	9
IV	TRAFFIC MODELLING Types of traffic models – need for traffic models – traffic model types - Little’s theorem, Need for modeling, Poisson modeling and its failure, Non- poisson models, Network performance evaluation.	9
V	NETWORK SECURITY AND MANAGEMENT Principles of cryptography – Authentication – integrity – key distribution and certification – Access control and: fire walls – attacks and counter measures – security in many layers. Infrastructure for network management – The internet standard management framework – SMI, MIB, SNMP, Security and administration – ASN.1-RMON- Network management tools	9
Total instructional hours		45

- Course Outcome
- CO1: Gain the knowledge of multimedia networking.
 - CO2: Understand the advanced networking concepts.
 - CO3: Familiarizes the network security and management.
 - CO4: Impart the knowledge of advanced network securities.
 - CO5: Discuss about the network management.


TEXT BOOKS:

- T1. J.F. Kurose & K.W. Ross, "Computer Networking- A top down approach featuring the internet", Pearson, 2nd edition, 2003.
- T2. Walrand J. Varatya, High performance communication network, Morgan Kauffman – Harcourt Asia Pvt. Ltd, 2nd Edition, 2000.

REFERENCE BOOKS:

- R1. LEOM-GarCIA, WIDJAJA, "Communication networks", TMH seventh reprint 2002.
- R2. Aunurag kumar, D. M Anjunath, Joy kuri, "Communication Networking", Morgan Kaufmann Publishers, 1ed 2004.
- R3. Hersent Gurle & petit, "IP Telephony, packet Pored Multimedia communication Systems", Pearson education 2003.




Chairman - BoS
EEE - HICET


Dean (Academics)
HICET

PROGRAMME	COURSE CODE	NAME OF THE COURSE	L	T	P	C
M.E.	16AP2310	INDUSTRIAL AUTOMATION AND CONTROL	3	0	0	3

- Course Objective
1. Understand principles of switching theory and switching elements (pneumatics and hydraulics).
 2. Study different types of sensors and transducers.
 3. Familiarize the architecture of PLC, PLC Ladder diagrams, types of PLC and their installation.
 4. Impart knowledge on types of DCS.
 5. Understand the basic principles of electric, Hydraulic and Pneumatic control systems

Unit	Description	Instructional hours
I	SWITCHING THEORY AND SWITCHING ELEMENTS Basic logic gates, Binary elements and variables, logic circuit design. Switching elements: electronic logic gates- relays – pneumatic valves- MPL elements – solenoid valves- interfacing pneumatics and hydraulics.	9
II	SENSORS AND TRANSDUCERS Binary vs. analog sensors – electric position sensors – pneumatic position sensors – point sensors for variables other than position. Electrical transducers – selection of transducer-final control elements.	9
III	FLEXIBLE AUTOMATION Programmable logic controllers (PLC) – programming-ladder diagram- PLC communication and networking- PLC selection and installation- examples of PLC applications.	9
IV	DISTRIBUTED CONTROL SYSTEM Introduction to DCS- DCS Integrated with PLC and computer system- computer aided measurement and control system- elements and architecture of computer aided measurement and control system- MMI- communication and networking- data transfer techniques- RTO's – computer based data acquisition system (DAQ).	9
V	APPLICATIONS OF CONTROL SYSTEM Basic Principles of electric, Hydraulic and Pneumatic control systems-Electric oven temperature control-Automatic control of metal width and thickness.	9
Total instructional hours		45

- Course Outcome
- CO1: Apply the principles of pneumatics and hydraulics and analyze their interference system.
CO2: Recall the applications of various sensors and transducers.
CO3: Draw ladder diagrams for given applications.
CO4: Construct and analyze DCS integrated with PLC
CO5: Write PLC program for temperature control in an electric oven.

TEXT BOOKS:

- T1. M.P.Groover, "Automation, Production Systems and Computer Integrated manufacturing", Pearson Education 5th edition, 2009
T2. David W Pessen, "Industrial Automation Circuit Design and Components", John Wiley & Sons 2011.

REFERENCE BOOKS:

- R1. S.K.Singh, "Industrial Instrumentation and Control", Tata Mc Graw Hill Education Pvt. Ltd. 2012.
R2. Gary Dunning, "Introduction to Programmable Logic Controllers", Delmar Publisher.
R3. Webb & Resis, "Programmable Logic Controllers", Prentice Hall of India 2000



[Signature]
Chairman - BoS
EEE - HICET

[Signature]
Dean (Academics)
HICET

PROFESSIONAL ELECTIVE V

PROGRAMME	COURSE CODE	NAME OF THE COURSE	L	T	P	C
M.E.	16AP3301	TESTING OF VLSI CIRCUITS	3	0	0	3

- Course Objective
1. Infer basic concepts on testing of VLSI circuits.
 2. Recall the basics of combinational and sequential circuits.
 3. Gain knowledge on testing of logic circuits.
 4. Learn algorithms for testing the logical circuits.
 5. Diagnose the faults in combinational and logic circuits.

Unit	Description	Instructional Hours
	TESTING AND FAULT MODELLING	
I	Introduction to testing – Faults in Digital Circuits – Modelling of faults – Logical Fault Models – Fault detection – Fault Location – Fault dominance – Logic simulation – Types of simulation – Delay models – Gate Level Event – driven simulation.	9
	TEST GENERATION FOR COMBINATIONAL AND SEQUENTIAL CIRCUITS	
II	Test generation for combinational logic circuits – Testable combinational logic circuit design – Test generation for sequential circuits – design of testable sequential circuits.	9
	DESIGN FOR TESTABILITY	
III	Design for Testability – Ad-hoc design – Generic scan based design – Classical scan based design – System level DFT approaches.	9
	SELF – TEST AND TEST ALGORITHMS	
IV	Built-In self Test – Test pattern generation for BIST – Circular BIST – BIST Architectures – Testable Memory Design – Test Algorithms – Test generation for Embedded RAMs.	9
	FAULT DIAGNOSIS	
V	Logical Level Diagnosis – Diagnosis by UUT reduction – Fault Diagnosis for Combinational Circuits – Self-checking design – System Level Diagnosis.	9
Total Instructional Hours		45

- Course Outcome
- CO1: Design models of various fault diagnosis circuits.
 CO2: Construct test circuit for combinational and sequential processes.
 CO3: Analyze the various test generation methods for logic circuits.
 CO4: Employ the appropriate design algorithm for constructing logic circuits.
 CO5: Suggest suitable circuit for fault diagnosis.


TEXT BOOKS:

- T1. M.Abramovici, M.A.Breuer and A.D. Friedman, “Digital systems and Testable Design”, Jaico Publishing House, 2002.
- T2. P.K. Lala, “Digital Circuit Testing and Testability”, Academic Press, 2002.

REFERENCE BOOKS:

- R1. M.L.Bushnell and V.D.Agrawal, “Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits”, Kluwer Academic Publishers, 2002.
- R2. A.L.Crouch, “Design Test for Digital IC’s and Embedded Core Systems”, Prentice Hall International, 2002.




Chairman - BoS
EEE - HiCET


Dean (Academics)
HiCET

PROGRAMME	COURSE CODE	NAME OF THE COURSE	L	T	P	C
M.E.	16AP3302	PHOTONICS	3	0	0	3

- Course Objective
1. Gain knowledge on light and its propagation.
 2. Analyze the performance of bistable LASER diodes.
 3. Distinguish the performance issues in LASER diodes.
 4. Design electronic circuits for wavelength selection and photo detection.
 5. Propose suitable applications for photonic switching.

Unit	Description	Instructional Hours
	INTRODUCTION	
I	Function semiconductor laser - Basic concepts of semi conductor laser - Semi conductor quantum wells - Vertical cavity surface emitting lasers - Non linear effects in semiconductor lasers.	9
	BISTABLE LASER DIODES	
II	Optical Bistability - Bistable switches - Inhomogeneous current injections – absorptive scheme - Dispersive bistable laser diodes - Injection locking - Bistability in laser diode amplifiers - wavelength, power and polarization bistability.	9
	SELF PULSATION & ULTRA SHORT PULSE GENERATORS	
III	Self pulsation-theory of self pulsation in laser diodes, Period doubling in modulated laser diodes - Optical chaos - Mode locking in laser diodes - Monolithic mode locked laser diodes.	9
	WAVELENGTH SELECTION AND WAVELENGTH SELECTIVE PHOTODETECTION	
IV	Wavelength selection - Laser diode amplifier filters - DFB laser diode amplifier - Signal selection, Noise properties and Wavelength selection photo detectors.	9
	APPLICATIONS OF PHOTONIC SWITCHING	
V	High speed data transmission systems - Clock distribution - All optical fibre communication systems - Clock extraction & dispersion compensation - WDM systems - optical exchange systems - Time division & wavelength division switching - Power mixing & Frequency division switching - Space switches.	9
Total Instructional Hours		45

- Course Outcome
- CO1: Elaborate the performance issues in various LASERS.
CO2: Suggest suitable application for bistable LASER diodes.
CO3: Appraise the solutions for the performance issues in LASER diodes.
CO4: Adapt the suitable circuit for wavelength selection, detection and photo detection.
CO5: Evaluate the applications of photonic switching.

TEXT BOOKS:

- T1. H. Kawaguchi, "Bistabilities and Non-linearities in Laser Diodes", Artech house Inc, Norwood, 1994.
T2. Saleh, B. E. A., and M. C. Teich., "Fundamentals of Photonics", New York, NY: Wiley, 1991.

REFERENCE BOOKS:

- R1. Sueta and Okoshi, "Fundamental of Ultra fast & Ultra Parallel Opto Electronics", John Wiley & Sons, New York, 1996.
R2. K. Tada and Hinton. H.S., "Photonic Switching II", Springer Verlag, Berlin, 1990.



[Signature]
Chairman - BoS
EEE - HICET

[Signature]
Dean (Academics)
HICET

PROGRAMME	COURSE CODE	NAME OF THE COURSE	L	T	P	C
M.E.	16AP3303	NANO ELECTRONICS	3	0	0	3

- Course Objective
1. Learn the basics of various dimensional nanostructures.
 2. Analyze various properties of nanostructure.
 3. Understand the importance of quantum dots in nano structures.
 4. Infer the basics of nano structure devices.
 5. Design application circuits using nano structures.

Unit	Description	Instructional Hours
	INTRODUCTION	
I	Electronic states in crystal energy bands - 1 D nanostructures (quantum wires) - OD nanostructures (quantum dots) - Concepts of 2 and 3D nanostructures (quantum wells), artificial atomic clusters.	9
	FABRICATION AND MEASUREMENT TECHNIQUES	
II	Size dependent properties - Size dependent absorption spectra - Blue shift with smaller sizes - Phonons in nanostructures - Contacts at Nano level – AFM (classification) - ISTM tip on a surface.	9
	PROPERTIES	
III	Charging of quantum dots - Coulomb blockade - Quantum mechanical treatment of quantum wells - wires and dots - Widening of band gap in quantum dots - Strong and weak confinement - Properties of coupled quantum dots - Optical scattering from Nano defects.	9
	NANO STRUCTURE DEVICES	
IV	Nano composites – Ceramic - Polymer and metal material composites - Electronic and atomic structure of aggregates and nano particles - Theory and modeling of nano particles fictionalization processes - organic electronics.	9
	LOGIC DEVICES AND APPLICATIONS	
V	Nano systems -Synthesis and characterization methods - Molecular beam epitaxy - MOCVD - chemical routes - nano particles of polymers - pulsed laser deposition - ion beam assisted techniques including embedded nano particles - RF sputtering. -Inert gas condensation.	9
Total Instructional Hours		45

- Course Outcome
- CO1: Summarize the concepts on various dimensional nanostructures.
CO2: Compile the properties of nanostructure.
CO3: Recognize the basics of nanostructure devices and logic devices.
CO4: Compile the performance of nano structure devices.
CO5: Categories the application circuits of nano structures.

TEXT BOOKS:

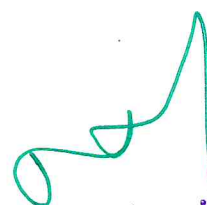
- T1. K.Bamam and D.Vvedensky “Low Dimensional Semiconductor Structures”, Cambridge University Book, 2001.
T2. L.Banyai and S.W.Koch, “Semiconductor Quantum Dots”, World Scientific, 1993.

REFERENCE BOOKS:

- R1. J.H. Davies, “An introduction to the physics-a low dimensional semiconductors”, Cambridge Press, 1998.
R2. Karl Gosser, Peter Glosekotter, Jan Dienstuhl., “Nanoelectronics and Nanosystems”, Springer, 2004.


Chairman - BoS
EEE - HICET




Dean (Academics)
HICET

PROGRAMME	COURSE CODE	NAME OF THE COURSE	L	T	P	C
M.E.	16AP3304	INTERNETWORKING AND MULTIMEDIA	3	0	0	3

- Course Objective
1. Identify and analyze the requirements of multimedia communication network.
 2. Infer the basics of broad band technology.
 3. Learn the basics of reliable transport protocols.
 4. Infer about various multimedia communication standards and architectures.
 5. Analyze the process involved in data transmission across various networks.

Unit	Description	Instructional Hours
	MULTIMEDIA NETWORKING	
I	Digital Sound, Video and Graphics – Basic Multimedia Networking – Multimedia Characteristics – Evolution of Internet Services Model – Network Requirements for Audio/ Video Transform – Multimedia Coding and Compression for Text, Image Audio And Video.	9
	BROADBAND NETWORK TECHNOLOGY	
II	Broadband Services – ATM and IP, IPV6, High Speed Switching – Resource Reservation - Buffer Management – Traffic Shaping – Caching – Scheduling and Policing – Throughput - Delay and Jitter Performance – Storage and Media Services – Voice and Video over IP – MPEG-2 over ATM/IP – Indexing Synchronization of Requests – Recording and Remote Control .	9
	RELIABLE TRANSPORT PROTOCOL AND APPLICATIONS	
III	Multicast over Shared Media Network – Multicast Routing and Addressing – Scaling Multicast and NBMA Networks – Reliable Transport Protocols – TCP Adaptation Algorithm – RTP - RTCP – MIME – Peer-to-Peer Computing – Shared Application – SIP - SDP.	9
	MULTIMEDIA COMMUNICATION STANDARDS	
IV	Objective of MPEG – 7 Standards – Functionalities and Systems of MPEG-7 MPEG-21 Multimedia Framework Architecture – Content Representation – Content Management and Usage – Intellectual Property Management – Audio Visual System – H264: Guaranteed QOS LAN Systems – MPEG_4 Video Transport Across Internet.	9
	MULTIMEDIA COMMUNICATION ACROSS NETWORKS	
V	Packet Audio/Video in The Network Environment –Video Transport Across Generic Networks – Layered Video Coding– Error Resilient Video Coding Techniques – Scalable Rate Control – Streaming Video Across Internet – Multimedia Transport Across ATM Networks and IP Network – Multimedia Across Wireless Networks .	9

Total Instructional Hours 45

- Course Outcome
- CO1: Describe different realizations of multimedia tools and the way in which they are used.
CO2: Summarize the structure of broad band techniques and its associated standards.
CO3: Design a suitable application using reliable transport protocols.
CO4: Compare and contrast different multimedia standards.
CO5: Discuss the data transfer process across various networks.

TEXT BOOKS:

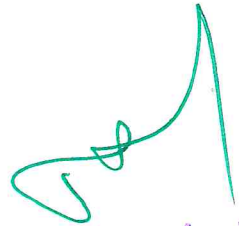
- T1. B. O. Szuprowicz, "Multimedia Networking", McGraw Hill, Newyork, 1995.
T2. K. R. Rao, Zoran S, Bojkovic and Dragorad A, Milovanovic "Multimedia communication systems", PHI, 2003.

REFERENCE BOOKS:

- R1. Jon Crowcroft, Mark Handley, Ian Wakeman "Internetworking Multimedia" Harcourt, Singapore, 1998.
R2. Tay Vaughan, "Multimedia making it to work", 4th edition Tata McGraw Hill, New Delhi, 2000.


Chairman - BoS
EEE - HICET




Dean (Academics)
HICET

PROGRAMME	COURSE CODE	NAME OF THE COURSE	L	T	P	C
M.E.	16AP3305	ASIC DESIGN	3	0	0	3

- Course Objective
1. Study the design flow of different types of ASIC.
 2. Discuss the architecture of ASIC.
 3. Gain knowledge on partitioning, floor planning, placement and routing including circuit extraction of ASIC.
 4. Learn about different high performance algorithms and its applications in ASICs.
 5. Infer about the partitioning and routing methods in ASIC circuits.

Unit	Description	Instructional Hours
I	INTRODUCTION TO ASICs, CMOS LOGIC AND ASIC LIBRARY DESIGN Types of ASICs - Design flow - CMOS transistors CMOS Design rules – Combinational Logic Cell – Sequential logic cell - Data path logic cell - Transistors as Resistors - Transistor Parasitic Capacitance- Logical effort –Library cell design - Library architecture.	9
II	PROGRAMMABLE ASICs, PROGRAMMABLE ASIC LOGIC CELLS AND programmable ASIC I/O cells anti fuse - static RAM - EPROM and EEPROM technology - PREP benchmarks - Actel ACT - Xilinx LCA –Altera FLEX - Altera MAX DC & AC inputs and outputs - Clock & Power inputs - Xilinx I/O blocks.	9
III	PROGRAMMABLE ASIC INTERCONNECT, PROGRAMMABLE ASIC DESIGN SOFTWARE AND LOW LEVEL DESIGN ENTRY Actel ACT -Xilinx LCA - Xilinx EPLD - Altera MAX 5000 and 7000 - Altera MAX 9000 - Altera FLEX –Design systems - Logic Synthesis - Half gate ASIC -Schematic entry – Low level design language - PLA tools -EDIF- CFI design representation.	9
IV	LOGIC SYNTHESIS, SIMULATION AND TESTING Verilog and logic synthesis -VHDL and logic synthesis - Types of simulation –Boundary scan test - fault simulation - Automatic test pattern generation.	9
V	ASIC CONSTRUCTION, FLOOR PLANNING, PLACEMENT AND ROUTING System partition - FPGA partitioning - partitioning methods - floor planning - placement - physical design flow –global routing - detailed routing - special routing - circuit extraction - DRC.	9
	Total Instructional Hours	45
Course Outcome	CO1: Analyze the characteristics and performance of ASICs and judge independently the best suited device for fabrication. CO2: Conducting research in ASIC design. CO3: Solve design issues and simulate and Test ASICs. CO4: Apply appropriate techniques, resources and tools to develop ASICs for engineering activities CO5: Design the ASIC circuit.	

TEXT BOOKS:

- T1. M.J.S .Smith, "Application Specific Integrated Circuits", Addison -Wesley Longman Inc., 1997.
- T2. Farzad Nekoogar and Faranak Nekoogar, "From ASICs to SOCs: A Practical Approach", Prentice Hall PTR, 2003.

REFERENCE BOOKS:

- R1. Wayne Wolf, "FPGA-Based System Design", Prentice Hall PTR, 2004.
- R2. Rajsuman, "System-on-a-Chip Design and Test", Santa Clara, CA: Artech House Publishers, 2000.
- R3. F. Nekoogar, "Timing Verification of Application-Specific Integrated Circuits (ASICs)", Prentice Hall PTR, 1999.


Chairman - BoS
EEE - HICET




Dean (Academics)
HICET

PROFESSIONAL ELECTIVE VI

PROGRAMME	COURSE CODE	NAME OF THE COURSE	L	T	P	C
M.E.	16AP3306	ROBOTICS	3	0	0	3

- Course Objective
1. Infer the fundamentals of robotics.
 2. Recall the concepts of vision system.
 3. Outline the working of sensor devices.
 4. Coding for developing robot using artificial intelligence techniques.
 5. Apply artificial intelligence algorithms to design robots.

Unit	Description	Instructional Hours
I	INTRODUCTION Robotic Classification, Robot Specifications, Motion – Bug and tangent algorithms, Potential Function, Road maps- Topological roadmaps, Cell decomposition – Trapezoidal and Morse cell decompositions , Sensor and sensor planning- Kinematics-Forward and Inverse Kinematics - Transformation matrix and DH transformation-Inverse Kinematics - Geometric methods and Algebraic methods.	9
II	COMPUTER VISION Projection – Optics - Projection on the Image Plane and Radiometry. - Image Processing – Connectivity - Images-Gray Scale and Binary Images - Blob Filling - Thresholding, Histogram-Convolution - Digital Convolution and Filtering and Masking Techniques- Edge Detection - Mono and Stereo Vision.	9
III	SENSORS AND SENSING DEVICES Introduction to various types of sensor- Resistive sensors. Range sensors - LADAR (Laser Distance and Ranging), Sonar, Radar and Infra-red- Introduction to sensing - Light sensing, Heat sensing, touch sensing and Position calculating by using mono-vision camera.	9
IV	ARTIFICIAL INTELLIGENCE Uniform Search strategies - Breadth first - Depth first - Depth limited - Iterative and deepening depth first search and Bidirectional search - algorithm- Planning - State-Space Planning Plan-Space Planning - Graph plan/Sat Plan and their Comparison - Multi-agent planning and Multi-agent planning - Probabilistic Reasoning - Bayesian Networks - Decision Trees and Bayes net inference .	9
V	INTEGRATION TO ROBOT Building of 4 axis or 6 axis robot - Vision System for pattern detection - Sensors for obstacle detection - AI algorithms for path finding and decision making.	9
Total Instructional Hours		45

- Course Outcome
- CO1: Illustrate the fundamentals of robots.
 CO2: Compile the concepts learnt about robotic vision system.
 CO3: Develop robots with differential motion and control.
 CO4: Build programs for robots in various applications.
 CO5: Identify the robotic applications with various axes.

TEXT BOOKS:

- T1. Duda, Hart and Stork, "Pattern Recognition", Wiley-Inter science, 2000.
 T2. Mallot, "Computational Vision: Information Processing in Perception and Visual Behavior", Cambridge, 2000.

REFERENCE BOOKS:

- R1. Stuart Russell and Peter Norvig, "Artificial Intelligence-A Modern Approach", Pearson Education Series in Artificial Intelligence, 2004.
 R2. Robert Schilling and Craig, "Fundamentals of Robotics: Analysis and Control", Hall of India Private Limited, 2003.
 R3. Forsyth and Ponce, "Computer Vision: A Modern Approach", Person Education, 2003.

[Signature]
Chairman - BoS
EEE - HICET



[Signature]
Dean (Academics)
HICET

PROGRAMME	COURSE CODE	NAME OF THE COURSE	L	T	P	C
M.E.	16AP3307	MEMS AND NEMS	3	0	0	3

- Course Objective
1. Learn the basics of micro electromechanical devices.
 2. Infer the fabrication process of Microsystems.
 3. Design MEMS sensor.
 4. Discuss about scaling and packaging issues in MEMS.
 5. Intend suitable application for MEMS.

Unit	Description	Instructional Hours
	OVERVIEW AND INTRODUCTION	
I	MEMS and NEMS – working principles - MEMS processes & features, various components of MEMS, applications and standards, micromachining, basic process tools – epitaxy – sputtering - chemical vapor deposition and spin on methods – oxidation – evaporation - lithography and etching - advanced process tools - sol gel process - EFAB.	9
	MATERIALS FOR MEMS AND ENGINEERING ASPECTS	
II	Silicon - Silicon oxide and nitride - Thin metal films – Polymers - Other materials and substrates - polycrystalline materials - mechanics of Microsystems - static bending -mechanical vibrations - thermo mechanics - fracture mechanism – fatigue - and stress and strain - young’s modulus and modulus of rigidity - scaling laws in miniaturization.	9
	MEMS SENSORS, DESIGN AND PROCESSING	
III	Micro sensors (acoustic wave sensors- biomedical sensors- chemical sensors- optical sensors- capacitive sensors- pressure sensors- thermal sensors) - micro actuators (thermal- piezoelectric- electrostatic actuators- micrometers- micro valves & pumps- accelerometer- micro fluidics and devices) - design consideration - process design and mechanical design.	9
	MEMS/NEMS SCALING ISSUES AND PACKAGING	
IV	Introduction – Scaling of physical systems – Mechanical system scaling, Thermal system scaling - Fluidic system scaling - Electrical system scaling - Packaging - mechanical and micro system package - design considerations - Process steps - Die preparation – interconnects - surface and Wafer bonding - wire bonding and scaling - 3D packaging and assembly signal Thermal management - Hermetic packaging, Electrical / Micro fluidic / and optical interconnects - Signal mapping transduction - Micro fluidic technology - MEMS and NEMS technology for micro fluidic devices.	9
	MEMS/NEMS APPLICATIONS	
V	Applications in automotive industry – health care – aerospace – industrial product consumer products – lab on chip – molecular machines – data storage devices – micro reactor – telecommunications - Servo systems.	9
	Total Instructional Hours	45

- Course Outcome
- CO1: Illustrate the fundamentals of MEMS.
CO2: Describe the materials used for MEMS.
CO3: Design and analysis of MEMS sensors and actuators.
CO4: Summarize MEMS / NEMS scaling issues and packaging.
CO5: Analysis the applications of MEMS.

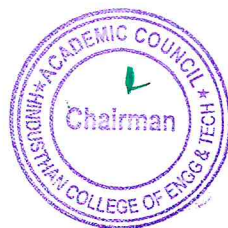
TEXT BOOKS:

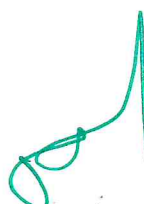
- T1. Nadim Malut and Kirt Williams, “An introduction to Micro electro mechanical systems Engineering”, Artech House Inc, Boston, Second edition, 2004.
T2. James J Allen, “Micro electro mechanical systems Design”, CRC Press, Taylor and Francis Group, 2001.

REFERENCE BOOKS:

- R1. Nicolae Lobontiu and Ephrahim Garcia Kluwer, “Mechanics of micro electro mechanical systems”, Academic Publishers, Boston, 2001.
R2. Ivor Brodie and Julius J.Murray, “The Physics of Micro/Nano – Fabrication”, Springer Science & Business Media, 2013.
R3. Kaoru Ohno, Masatoshi Tanaka, Jun Takeda and Yoshijuki Kawazoe, “Nano - and Micromaterials”, Springer Science & Business Media, 2008.


Chairman - BoS
BEE - HICET




Dean (Academics)
HICET

PROGRAMME	COURSE CODE	NAME OF THE COURSE	L	T	P	C
M.E.	16AP3308	SYSTEM ON CHIP DESIGN	3	0	0	3

- Course Objective
1. Learn about designing various logic gates with minimum size, spacing, and parasitic values.
 2. Design combinational logic functions and analyze delay and testability properties of interconnect and gates.
 3. Correlate optimization of power in sequential logic machines.
 4. Study the design principles of FPGA and PLA.
 5. Learn various floor planning methods for system design.

Unit	Description	Instructional Hours
I	LOGIC GATES Introduction- Combinational Logic Functions- Static Complementary Gates- Switch Logic- Alternative Gate Circuits- Low - Power Gates- Delay Through Resistive Interconnect - Delay Through Inductive Interconnect.	9
II	COMBINATIONAL LOGIC NETWORKS Introduction- Standard Cell - Based Layout- Simulation- Combinational Network Delay- Logic and interconnect Design- Power Optimization- Switch Logic Networks- Combinational Logic Testing.	9
III	SEQUENTIAL MACHINES Introduction- Latches and Flip - Flops- Sequential Systems and Clocking Disciplines- Sequential System Design- Power Optimization- Design Validation- Sequential Testing.	9
IV	SUBSYSTEM DESIGN Introduction- Subsystem Design Principles- Combinational Shifters- Adders- ALUs- Multipliers- High - Density Memory- Field Programmable Gate Arrays- Programmable Logic Arrays- References- Problems.	9
V	FLOOR-PLANNING Introduction - Floor - planning Methods – Block Placement & Channel Definition- Global Routing- switchbox Routing- Power Distribution- Clock Distributions- Floor - planning Tips- Design Validation- Off - Chip Connections – Packages- The I/O Architecture- and PAD Design.	9
Total Instructional Hours		45


- Course Outcome
- CO1: Design logic gates with minimum size, spacing, and parasitic values.
CO2: Suggest suitable design for logic gates with minimum size, spacing, and parasitic values.
CO3: Design combinational logic machines with optimum power.
CO4: Learn the design principles of FPGA and PLA.
CO5: Suggest various floor planning methods for system design.

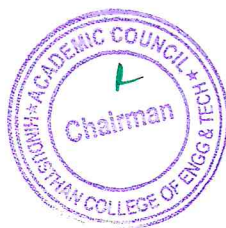
TEXT BOOKS:


- T1. Wayne Wolf, "Modern VLSI Design – System – on – Chip Design", Prentice Hall, 3rd Edition, 2008.
T2. Michael J. Flynn, Wayne Luk, "Computer System Design: System-on-Chip", Wiley Publications, 2003.

REFERENCE BOOKS:

- R1. Michel Robert, Bruno Rouzeyre, Christian Pigué, Marie-Lise Flottes, "SOC Design Methodologies", Springer Science & Business Media, 2001.
R2. Steve Furber, "Arm System-On-Chip Architecture", second edition, Pearson Education India, 2002
R3. Peter J. Ashenden, Jean Mermet, Ralf Seepold, "System-on-Chip Methodologies & Design Languages", Springer Science & Business Media, 2002.


Chairman - BoS
EEE - HICET




Dean (Academics)
HICET

PROGRAMME	COURSE CODE	NAME OF THE COURSE	L	T	P	C
M.E.	16AP3309	WIRELESS ADHOC AND SENSOR NETWORKS	3	0	0	3

- Course Objective
1. Develop an understanding of sensor network architectures from design and performance perspective.
 2. Learn different types of MAC protocols.
 3. Infer basics of adhoc routing protocols.
 4. Study the TCP issues in adhoc networks.
 5. Learn the architecture and protocols of wireless sensor networks.

Unit	Description	Instructional Hours
	INTRODUCTION	
I	Fundamentals of Wireless Communication Technology – The Electromagnetic Spectrum – Radio propagation Mechanisms – Characteristics of the Wireless Channel -mobile ad hoc networks (MANETs) and wireless sensor networks (WSNs): concepts and architectures. Applications of Ad Hoc and Sensor networks. Design Challenges in Ad hoc and Sensor Networks.	9
	MAC PROTOCOLS FOR AD HOC WIRELESS NETWORKS	
II	Issues in designing a MAC Protocol- Classification of MAC Protocols- Contention based protocols- Contention based protocols with Reservation Mechanisms- Contention based protocols with Scheduling Mechanisms – Multi channel MAC-IEEE 802.11	9
	ROUTING PROTOCOLS AND TRANSPORT LAYER IN AD HOC WIRELESS NETWORKS	
III	Issues in designing a routing and Transport Layer protocol for Ad hoc networks- proactive routing, Reactive routing (on-demand), hybrid routing- Classification of Transport Layer solutions-TCP over Ad hoc wireless Networks.	9
	WIRELESS SENSOR NETWORKS (WSNS) AND MAC PROTOCOLS	
IV	Single node architecture: hardware and software components of a sensor node - WSN Network architecture: typical network architectures-data relaying and aggregation strategies -MAC layer Protocols: self-organizing, Hybrid TDMA/FDMA and CSMA based MAC- IEEE 802.15.4.	9
	WSN ROUTING, LOCALIZATION & QOS	
V	Issues in WSN routing – OLSR- Localization – Indoor and Sensor Network Localization-absolute and relative localization, triangulation-QoS in WSN-Energy Efficient Design-Synchronization Transport Layer issues.	9
	Total Instructional Hours	45

- Course Outcome
- CO1: Identify different issues in wireless ad hoc and sensor networks.
CO2: Analyze protocols developed for ad hoc and sensor networks.
CO3: Identify and understand security issues in ad hoc and sensor networks.
CO4: Infer the architectures and security issues associated with multicast routing.
CO5: Evaluate the QoS related performance measurements of ad hoc and sensor networks.

TEXT BOOKS:

- T1. C.Siva Ram Murthy and B.S.Manoj, "Ad Hoc Wireless Networks – Architectures and Protocols", Pearson Education, 2004.
- T2. Carlos De Moraes Cordeiro, Dharma Prakash Agrawal, "Ad Hoc and Sensor Networks: Theory and Applications (2nd Edition)", World Scientific Publishing, 2011.

REFERENCE BOOKS:

- R1. Holger Karl, Andreas Willig, "Protocols and Architectures for Wireless Sensor Networks", John Wiley & Sons, Inc., 2005.
- R2. C.K.Toh, "Ad Hoc Mobile Wireless Networks", Pearson Education, 2009.
- R3. Subir Kumar Sarkar, T G Basavaraju, C Puttamadappa, "Ad Hoc Mobile Wireless Networks", Auerbach Publications, 2008.



[Signature]
Chairman - BoS
EEE - HiCET

[Signature]
Dean (Academics)
HiCET

PROGRAMME	COURSE CODE	NAME OF THE COURSE	L	T	P	C
M.E.	16AP3310	APPLIED MEDICAL IMAGE PROCESSING	3	0	0	3

- Course Objective
1. Learn the fundamentals of medical image processing techniques.
 2. Discuss about various medical imaging techniques.
 3. Gather knowledge on various forms of representation of medical images.
 4. Classify the ways of representing medical images.
 5. Infer methods of medical image visualization.

Unit	Description	Instructional Hours
	IMAGE FUNDAMENTALS AND PRE-PROCESSING	
I	Image perception- MTF of the visual system- Image fidelity criteria- Image model- Image sampling and quantization – Two dimensional sampling theory- Image quantization- Optimum mean square quantizer- Image transforms – 2D-DFT and other transforms. Image enhancement – point operation- Histogram modeling- spatial operations- Transform operations.	9
	BASICS OF MEDICAL IMAGE SOURCES	
II	Radiology- The electromagnetic spectrum-Computed Tomography - Magnetic Resonance Tomography – ultrasound-nuclear medicine and molecular imaging-radiation protection and dosimetry.	9
	MEDICAL IMAGE REPRESENTATION	
III	Pixels and voxels – algebraic image operations - gray scale and color representation- depth-color and look up tables - image file formats- DICOM- other formats- Analyze 7.5 - NifTI and Interfile - Image quality and the signal to noise ratio- MATLAB based simple operations.	9
	MEDICAL IMAGE ANALYSIS AND CLASSIFICATION	
IV	Image segmentation- pixel – edge - region based segmentation - Image representation and analysis- Feature extraction and representation- Statistical-Shape- Texture- feature and image classification – Statistical- Rule based- Neural Network approaches.	9
	IMAGE REGISTRATIONS AND VISUALIZATION	
V	Rigid body visualization- Principal axis registration- Interactive principal axis registration- Feature based registration- Elastic deformation based registration- Image visualization – 2D display methods- 3D display methods- virtual reality based interactive visualization.	9
	Total Instructional Hours	45


- Course Outcome
- CO1: Compile image processing concepts for medical images.
CO2: Suggest suitable imaging technique for health complications.
CO3: Point out the suitable form of storing the data.
CO4: Elaborate on various analysis of medical images.
CO5: Select suitable method for medical image visualization.

TEXT BOOKS:

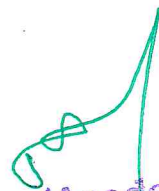
- T1. Wolfgang Birkfellner, “Applied Medical Image Processing – A Basic course”, CRC Press, 2011.
T2. Atam P.Dhawan, “Medical Image Analysis”, Wiley Interscience Publication, NJ, USA 2003.

REFERENCE BOOKS:

- R1. R.C.Gonzalez and R.E.Woods, “Digital Image Processing”, Second Edition, Pearson Education, 2002.
R2. Anil. K. Jain, “Fundamentals of Digital Image Processing”, Pearson education, Indian Reprint 2003.
R3. Alfred Horowitz, “MRI Physics for Radiologists – A Visual Approach”, Second edition, Springer Verlag Network, 1991.


Chairman - BoS
EEE - HICET




Dean (Academics)
HICET