HINDUSTHAN COLLEGE OF ENGINEERING AND TECHNOLOGY

(An Autonomous Institution Affiliated to Anna University, Chennai)

(AICTE, New Delhi, Accredited by NAAC with 'A' Grade)

COIMBATORE 641 032

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

M.E. APPLIED ELECTRONICS

Revised Curriculum and Syllabus for the Academic Year 2023-2024

I TO IV SEMESTERS CURRICULUM AND SYLLABI

SEMESTER I

S.No.	Course Code	Course Title	Category	L	T	P	C	CIA	ESE	TOTAL
THEORY										
1	20MA1102	Advanced Mathematics For Electrical And Electronics Engineering	BS	3	0	0	3	40	60	100
2	20AE1201	Advanced Digital System Design	PC	3	0	0	3	40	60	100
3	20AE1202	Embedded System Design	PC	3	0	0	3	40	60	100
4	20AE1203	Digital Image Processing	PC	3	0	0	3	40	60	100
5	20AE1204	Research Methodology	PC	3	0	0	3	40	60	100
6	20AC10XX	AUDIT COURSE I		2	0	0	0			
PRACTICAL										
7	20AE1001	Electronic System Design Laboratory	PC	0	0	4	2	50	50	100
8	20AE1002	Embedded System Laboratory	PC	0	0	4	2	50	50	100
MANDATORY COURSE										
Total Credits:				**17**	**00**	**08**	**19**			

SEMESTER II

S.No.	Course Code	Course Title	Category	L	T	P	C	CIA	ESE	TOTAL
THEORY										
1	20AE2201	Analog Integrated Circuit Design	PC	3	0	0	3	40	60	100
2	20AE2202	VLSI Design Techniques	PC	3	0	0	3	40	60	100
3	20AE23XX	**Professional Elective I**	PE	3	0	0	3	40	60	100
4	20AE23XX	**Professional Elective II**	PE	3	0	0	3	40	60	100
5	20AE23XX	**Professional Elective III**	PE	3	0	0	3	40	60	100
6	20AC20XX	AUDIT COURSE II		2	0	0	0			
PRACTICAL										
7	20AE2001	VLSI Design Laboratory	PC	0	0	4	2	50	50	100
8	20AE2901	MINI PROJECT	PC	2	0	0	2	50	50	100
Total Credits:				**19**	**00**	**08**	**19**			

SEMESTER III

S.No.	Course Code	Course Title	Category	L	T	P	C	CIA	ESE	TOTAL
THEORY										
1	20AE33XX	**Professional Elective IV**	PE	3	0	0	3	40	60	100
2	20AE33XX	**Professional Elective V**	PE	3	0	0	3	40	60	100
3	20AE34XX	**OPEN ELECTIVE**	OE	3	0	0	3	40	60	100
PRACTICAL										
4	20AE3901	DISSERTATION I	PC	0	0	20	10	50	50	100
Total Credits:				**09**	**00**	**20**	**19**			

SEMESTER IV

S.No.	Course Code	Course Title	Category	L	T	P	C	CIA	ESE	TOTAL
PRACTICAL										
1	20AE4901	DISSERTATION - II	PC	0	0	30	15	50	50	100
Total Credits:				0	0	30	15			

Total No of Credits: 72

LIST OF PROFESSIONAL ELECTIVES

Second Semester- (List of Professional Electives I, II, III)

S.No.	Course Code	Course Title	Category	L	T	P	C	CIA	ESE	TOTAL
1.	20AE2303	ASIC and FPGA Design	PE	3	0	0	3	40	60	100
2.	20AE2304	Physical Design of VLSI circuits	PE	3	0	0	3	40	60	100
3.	20AE2308	Wireless Adhoc and Sensor Networks	PE	3	0	0	3	40	60	100
4.	20AE2310	Satellite Communication and Navigation	PE	3	0	0	3	40	60	100
5.	20AE2313	Machine Learning	PE	3	0	0	3	40	60	100
6.	20AE2315	PCB Design and Fabrication	PE	3	0	0	3	40	60	100
7.	20AE2316	Testing of VLSI Circuits	PE	3	0	0	3	40	60	100
8.	20AE2317	Low Power VLSI Design	PE	3	0	0	3	40	60	100
9.	20AE2318	System on Chip Design	PE	3	0	0	3	40	60	100
10.	20AE2319	Cognitive Radio Network	PE	3	0	0	3	40	60	100

Third Semester (List of Professional Electives IV, V)

S.No.	Course Code	Course Title	Category	L	T	P	C	CIA	ESE	TOTAL
1.	20AE3301	Intelligent Systems and Control	PE	3	0	0	3	40	60	100
2.	20AE3302	Advanced Microprocessors and Microcontrollers	PE	3	0	0	3	40	60	100
3.	20AE3305	High Speed Switching and Network	PE	3	0	0	3	40	60	100
4.	20AE3306	Programming Languages for Embedded Software	PE	3	0	0	3	40	60	100
5.	20AE3309	Robotics and Intelligent Systems	PE	3	0	0	3	40	60	100
6.	20AE3311	5G Technology	PE	3	0	0	3	40	60	100
7.	20AE3312	IOT System Design and Security	PE	3	0	0	3	40	60	100
8.	20AE3314	Electronics for Solar Power	PE	3	0	0	3	40	60	100
9.	20AE3319	Nanoelectronics	PE	3	0	0	3	40	60	100
10.	20AE3320	Mems	PE	3	0	0	3	40	60	100

OPEN ELECTIVE

S.No.	Course Code	Course Title	Category	L	T	P	C	CIA	ESE	TOTAL
1	20AE3401	Robotics	OE	3	0	0	3	40	60	100
2	20AE3402	Artificial intelligence and Optimization Techniques	OE	3	0	0	3	40	60	100

AUDIT COURSES – I

S.No.	Course Code	Course Title	L	T	P	C
1	20AC1091	English for Research Paper writing	2	0	0	0
2	20AC1092	Disaster Management	2	0	0	0
3	20AC1093	Sanskrit for Technical knowledge	2	0	0	0
4	20AC1094	Value Education	2	0	0	0
5	20AC1095	Constitution of India	2	0	0	0

AUDIT COURSES - II

S.No.	Course Code	Course Title	L	T	P	C
1	20AC2091	Pedagogy Studies	2	0	0	0
2	20AC2092	Stress Management by Yoga	2	0	0	0
3	20AC2093	Personality Development Through Life Enlightenment Skills	2	0	0	0
4	20AC2094	Unnat Bharat Abhiyan	2	0	0	0

CREDIT DISTRIBUTION

Semester	I	II	III	IV	TOTAL
Credits	19	19	19	15	72

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SEMESTER-I

PROGRAMME	COURSE CODE	NAME OF THE COURSE	L	T	P	C
M.E	20MA1102	ADVANCED MATHEMATICS FOR ELECTRICAL AND ELECTRONICS ENGINEERING	3	0	0	3

Course Objective

1. Apply testing of hypothesis to infer outcome of experiments.
2. Formulate and construct a mathematical model for a linear programming problem in real life situation.
3. Understand the network modeling for planning and scheduling the project activities.
4. Develop the ability to use the concepts of Linear Algebra and Special functions for
5. Acquire knowledge of Fuzzy logic and Fuzzy Algebra.

Unit	Description	Instructional Hours
I	**TESTING OF HYPOTHESES** Sampling distributions -Type I and Type II errors - Tests based on Normal, t, Chi-Square and F distributions for testing of mean, variance and proportions -Tests for Independence of attributes and Goodness of fit.	9
II	**LINEAR PROGRAMMING** Formulation - Graphical solution - Simplex method - Artificial variable Techniques - Transportation and Assignment Models	9
III	**SCHEDULING BY PERT AND CPM** Network Construction - Critical Path Method - Project Evaluation and Review technique - Resource Analysis in Network Scheduling.	9
IV	**LINEAR ALGEBRA** Vector spaces – norms - Inner Products - Eigen values using QR Factorization - generalized eigenvectors - Canonical forms - singular value decomposition and applications -pseudo inverse - least square approximations -Toeplitz matrices and some applications.	9
V	**FUZZY LOGIC AND FUZZY ALGEBRA** Basic principles of Fuzzy logic - Fuzzy sets of operations - Fuzzy membership Matrix.	9
	Total Instructional Hours	**45**

Course Outcome

CO1:Acquire the basic concepts of Probability and Statistical techniques for solving mathematical problem which will be useful in solving engineering problems.
CO2:Apply transportation and assignment models to find optimal solution in warehousing and travelling.
CO3:Prepare project scheduling using PERT and CPM.
CO4:Achieve an understanding of the basic concepts of algebraic equations and method of solving
CO5:Apply the Fuzzy logic in power system problems.

TEXT BOOK

T1 -Richard Bronson, Gabriel B.Costa, "Linear Algebra", Academic Press, Second Edition,2007.
T2 -Richard Johnson, "Miller & Freund's Probability and Statistics for Engineer", Prentice –Hall, 7th Edition, 2007.
T3 - Taha H.A,"Operations Research, An Introduction "8th Edition, Pearson Education, 2008.

REFERENCE BOOKS

R1 -Gupta S.C. and Kapoor V.K."Fundementals of Mathematical Statistics", Sultan an Sons,2001.
R2 -Prem Kumar Gupta,D.S.Hira,"Operations Research," S.Chand &Company Ltd, New Delhi,3rd edition,2008.
R3- Panner Selvam,Operations Research",Prentice Hall of India,2002.
R4- George J.Klir and Yuan,B., Fuzzy sets and fuzzy logic, Theory and applications, Prentice Hall of India Pvt.Ltd., 1997.

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PROGRAMME	COURSE CODE	NAME OF THE COURSE	L	T	P	C
M.E	20AE1201	ADVANCED DIGITAL SYSTEM DESIGN	3	0	0	3

Course Objective

1. Basic concepts of Sequential Circuit Design.
2. Basic concepts of Asynchronous Sequential Circuit Design.
3. Learn the concepts of fault modeling and fault - tolerant systems
4. Study the concepts of programmable logic devices.
5. Apply the concepts of System Design Using Verilog and Programmable Devices

Unit	Description	Instructional Hours
I	**SEQUENTIAL CIRCUIT DESIGN** Analysis of clocked synchronous sequential circuits and modeling- State diagram, state table, state table assignment and reduction-Design of synchronous sequential circuits -ASM chart and realization using ASM.	9
II	**ASYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN** Analysis of asynchronous sequential circuit – flow table reduction-races-state assignment-transition table and problems in transition table- design of asynchronous sequential circuit-Static, dynamic and essential hazards – data synchronizers – mixed operating mode asynchronous circuits – designing vending machine controller	9
III	**FAULT DIAGNOSIS AND TESTABILITY ALGORITHMS** Fault table method-path sensitization method – Boolean difference method-D algorithm - Tolerance techniques – The compact algorithm – Fault in PLA – Test generation-DFT schemes – Built in self test.	9
IV	**SYNCHRONOUS DESIGN USING PROGRAMMABLE DEVICES** Programming logic device families – Designing a synchronous sequential circuit using PLA/PAL – Realization of finite state machine using PLD – FPGA – Xilinx FPGA-Xilinx 4000	9
V	**SYSTEM DESIGN USING VERILOG** Hardware Modelling with Verilog HDL – Logic System, Data Types and Operators For Modelling in Verilog HDL - Behavioral Descriptions in Verilog HDL – HDL Based Synthesis – Synthesis of Finite State Machines– structural modeling – compilation and simulation of Verilog code –Test bench - Realization of combinational and sequential circuits using Verilog – Registers – counters – sequential machine – serial adder – Multiplier- Divider – Design of simple microprocessor.	9
	Total Instructional Hours	**45**

Course Outcome

CO1: Design and analysis of sequential circuit.
CO2: Design and analysis of asynchronous sequential circuit.
CO3: Explore fault diagnosis and testability algorithm
CO4: Learn of programmable logic devices.
CO5: Design and analysis of hardware description languages.

TEXT BOOKS:

T1 Charles H.Roth Jr "Fundamentals of Logic Design" Thomson Learning 2004

T2 M.D.Ciletti , Modeling, Synthesis and Rapid Prototyping with the Verilog HDL, Prentice Hall, 1999.

REFERENCE BOOKS:

R1 M.G.Arnold, Verilog Digital – Computer Design, Prentice Hall (PTR), 1999.

R2 Parag K.Lala "Digital system Design using PLD" B S Publications,2003

R3 Nripendra N Biswas "Logic Design Theory" Prentice Hall of India,2001

R4 Parag K.Lala "Fault Tolerant and Fault Testable Hardware Design" B S Publications,2002

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PROGRAMME	COURSE CODE	NAME OF THE COURSE	L	T	P	C
M.E	20AE1203	DIGITAL IMAGE PROCESSING	3	0	0	3

COURSE OBJECTIVE

1. To understand the fundamentals of Digital Image
2. To analyze and design the Image transforms and Enhancement.
3. To study and analyze the operation of Image restoration and construction.
4. To study and understand the Image compression & Segmentation.
5. To understand color and multispectral image processing.

Unit	Description	Instructional Hours
I	**Digital Image Fundamentals.** Introduction: Digital Image- Steps of Digital Image Processing Systems-Elements of Visual Perception -Connectivity and Relations between Pixels. Simple Operations- Arithmetic, Logical, Geometric Operations. Mathematical Preliminaries - 2D Linear Space Invariant Systems - 2D Convolution - Correlation 2D Random Sequence - 2D Spectrum.	9
II	**Image Transforms and Enhancement.** Image Transforms: 2D Orthogonal and Unitary Transforms-Properties and Examples. 2D DFT-FFT – DCT -Hadamard Transform - Haar Transform - Slant Transform - KL Transform - Properties And Examples.Image Enhancement:- Histogram Equalization Technique- Point Processing-Spatial Filtering-In Space And Frequency - Nonlinear Filtering-Use Of Different Masks.	9
III	**Image restoration and construction.** Image Restoration: Image Observation And Degradation Model, Circulant And Block Circulant Matrices and Its Application In Degradation Model - Algebraic Approach to Restoration- Inverse By Wiener Filtering – Generalized Inverse-SVD and Interactive Methods - Blind Deconvolution-Image Reconstruction From Projections.	9
IV	**Image compression & segmentation** Image Compression: Redundancy And Compression Models -Loss Less And Lossy. Loss Less-Variable-Length, Huffman, Arithmetic Coding - Bit-Plane Coding, Loss Less Predictive Coding, LossyTransform (DCT) Based Coding, JPEG Standard - Sub Band Coding. Image Segmentation: Edge Detection - Line Detection - Curve Detection - Edge Linking And Boundary Extraction, Boundary Representation, Region Representation And Segmentation, Morphology-Dilation, Erosion, Opening And Closing. Hit And Miss Algorithms Feature Analysis	9
V	**Color and multispectral image processing** Color Image-Processing Fundamentals, RGB Models, HSI Models, Relationship Between Different Models. Multispectral Image Analysis - Color Image Processing Three Dimensional Image Processing-Computerized Axial Tomography-Stereometry-Stereoscopic Image Display-Shaded Surface Display.	9
	TOTAL INSTRUCTIONAL HOURS	**45**

COURSE OUTCOME

At the end of this course, students will be able to

CO1: Identify various arithmetic and geometrical operations of image fundamental.
CO2: Analyze the operation Image transforms and Enhancement.
CO3: Design Image compression and restoration techniques.
CO4: Design the Image compression and Segmentation.
CO5: Create models for color and multispectral image processing.

TEXT BOOKS:

T1 Digital Image Processing, Gonzalez.R.C & Woods. R.E., 3/e, Pearson Education, 2008.
T2 Digital Image Processing, Kenneth R Castleman, Pearson Education,1995.

REFERENCES:

R1 1. Digital Image Procesing, S. Jayaraman, S. Esakkirajan, T. Veerakumar, McGraw Hill Education ,2009
R2 2.Fundamentals of Digital image Processing, Anil Jain.K, Prentice Hall of India, 1989.
R3 3.Image Processing, Sid Ahmed, McGraw Hill, New York, 1995
R4 4.Image Processing: The Fundamentals, Maria Petrou,Costas Petrou,Wiley,2010

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PROGRAMME	COURSE CODE	NAME OF THE COURSE	L	T	P	C
M.E	20AE1202	EMBEDDED SYSTEM DESIGN	3	0	0	3

Course Objective

1. Understand the design challenges and methodologies of embedded system
2. Study general and single purpose processor and its developement
3. Understand bus structures
4. Learn the embedded system design procedurs for various processes
5. Study the embedded software tools for RTOS

Unit	Description	Instructional Hours
I	**EMBEDDED SYSTEM OVERVIEW** Embedded System Overview, Design Challenges – Optimizing Design Metrics, Design Methodology, RT-Level Combinational and Sequential Components, Optimizing Custom Single-Purpose Processors.	9
II	**GENERAL AND SINGLE PURPOSE PROCESSOR** Basic Architecture, Pipelining, Superscalar and VLIW architectures, Development Environment: Application-Specific Instruction-Set Processors (ASIPs) Microcontrollers, Timers, Counters and watchdog Timer, UART and Analog-to-Digital Converters, Memory Concepts.	9
III	**BUS STRUCTURES** Basic Protocol Concepts, Microprocessor Interfacing – I/O Addressing, Port and Bus-Based I/O, Arbitration, Serial Protocols, I^2C, CAN and USB, Parallel Protocols – PCI and ARM Bus, Wireless Protocols – IRDA, Bluetooth, IEEE 802.11.	9
IV	**STATE MACHINE AND CONCURRENT PROCESS MODELS** Basic State Machine Model, Finite-State Machine with Data path Model, Concurrent Process Model, Communication among Processes, Synchronization among processes, Dataflow Model, Real-time Systems, Automation: Synthesis, Intellectual Property Cores, Design Process Models.	9
V	**EMBEDDED SOFTWARE DEVELOPMENT TOOLS AND RTOS** Compilation Process – Libraries – Porting kernels – C extensions for embedded systems – Emulation and debugging techniques – RTOS – System design using RTOS.	9
	Total Instructional Hours	**45**

Course Outcome

CO1: Identify the various embedded system design
CO2: Evaluate the general and single purpose processors
CO3: Compare various bus structures
CO4: Recognize the process models
CO5: Apply the embedded software development tools

TEXT BOOKS:

T1 Bruce Powel Douglas, "Real time UML, second edition: Developing efficient objects for embedded systems", 3rd Edition 1999, Pearson Education.

T2 Frank Vahid and Tony Gwargie, "Embedded System Design", John Wiley & sons, 2002.

REFERENCE BOOKS:

R1 Daniel W.Lewis, "Fundamentals of embedded software where C and assembly meet", Pearson Education, 2002.

R2 Steve Heath, "Embedded System Design", Elsevier, Second Edition, 2004.

R3 Jonathan W.Valvano: "Embedded Microcomputer Systems – Real Time Interfacing", Cengage Learning; Third of later edition

R4 Osborn.G, "Embedded microcontroller and p0rocessor design", Pearson

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PROGRAMME	COURSE CODE	NAME OF THE COURSE	L	T	P	C
M.E	20AE1204	RESEARCH METHODOLOGY	3	0	0	3

Course Objectives

1. Impart scientific knowledge for carrying out research work effectively.
2. Understand the concepts in various research designs.
3. Acquire knowledge about Experimental design and Data collection
4. Confer about the multivariate analysis techniques
5. Disseminate knowledge on Research Practices and Report writing.

Unit	Description	Instructional hours
I	**INTRODUCTION TO RESEARCH** Research-Definition-Objectives of research, Meaning of research- Characteristics of research -Importance of research activities- Types of research-Research approaches-Significance-Problems in research- Qualities of good researcher- Research process.	9
II	**RESEARCH DESIGN** Formulation of the research design: Process-classification of research designs- Exploratory-Secondary resource analysis-Two-tired research design- -Validity in experimentation-factors affecting external validity-classification of experimental design - Pre-experimental- Quasi-experimental designs.	9
III	**DATA COLLECTION METHODS** Classification of Data-Collection of primary data-Observation-Interview method-Collection of data through Questionnaires-schedules-collection of secondary data-Research applications of secondary data-Benefits and drawbacks-classification of secondary data-Internal –External data sources.	9
IV	**MULTIVARIATE ANALYSIS TECHNIQUES** Growth of Multivariate techniques-Characteristics and applications-Classification-Variables in multivariate analysis-Important multivariate techniques-Factor analysis-Rotation in factor analysis-R-type and Q type factor analysis-Path analysis.	9
V	**RESEARCH PRACTICE AND REPORT WRITING.** Literature review-Conference proceedings-Journals-Journal Impact Factor (JFI)-Citation index-h-index-Significance of report writing-Different steps in writing report-Layout of report writing-Types of reports-Mechanics of writing a research report-precautions for writing research reports-Conclusion and Scope for future work-Oral presentation.	9
	Total instructional hours	**45**

Course Outcomes

CO1: Observe the various approaches to do research.
CO2: Carryout the research design.
CO3: Evaluate the data collection for research activities.
CO4: Acknowledge the function of Multivariate Analysis Techniques
CO5: Organize the research activity systematically and prepare research report effectively.

TEXT BOOKS:

T1. C.R. Kothari, Research Methodology Methods &Techniques, NEW Age International (P) Limited, New Delhi, 2007.

T2. Dr. Deepak Chawla, Dr. Neena Sondhi, Research Methodology concepts and cases, Vikas Publishing House Pvt. Ltd., New Delhi, 2011

REFERENCE BOOKS:

R1. K. Prathapan, Research Methodology for Scientific Research, I.K. International Publishing House Pvt. Ltd. New Delhi, 2014L.

R2. R. Panneerselvam, Research Methodology, PHI Learning Private Limited, New Delhi, 2011.

R3. Donald H. McBurney, Research Methods, Thomson Asia Pvt. Ltd. Singapore, 2002.

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PROGRAMME	COURSE CODE	NAME OF THE COURSE	L	T	P	C
M.E	20AE1001	ELECTRONIC SYSTEM DESIGN LABORATORY	0	0	4	2

Course Objective

1. Impart the knowledge on Interfacing of different Processor.
2. Testing of flash controller programming.
3. Analyze of process control and PCB designing.
4. Intend and analysis of modulator and demodulator.
5. Design system using instrumentation amplifier.

Expt. No.	Description of the experiments
1	Study of different interfaces (using Embedded Microcontroller).
2	Flash Controller Programming Data flash, with erase, verify and Fusing.
3	Design of Wireless Data Modem.
4	PCB layout design using CAD tool.
5	Design of Process Control Timer.
6	Design of AC/DC voltage regulator using SCR.
7	Design of an Instrumentation Amplifier.
8	Implementation of Adaptive filters and multistage multi-rate system in DSP processor.
9	Sensor design using simulation tools.
10	Design of Temperature sensor using Instrumentation Amplifier.

Total Practical Hours **45**

Course Outcome

CO1: Design various analog / digital transceiver systems and control different process.
CO2: Analyze flash controller programming and wireless data modem.
CO3: Analyze PCB designing for various circuits.
CO4: Propose interfaces using modulator and demodulator.
CO5: Design and analysis of operational and instrumentation amplifiers.

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PROGRAMME	COURSE CODE	NAME OF THE COURSE	L	T	P	C
M.E	20AE1002	EMBEDDED SYSTEMS LABORATORY	0	0	4	2

Course Objective

1. Impart the knowledge on various analog / digital transceiver systems and control different process.
2. Design system using 8086 and 8051 Microcontroller.
3. Study and design wireless network using embedded systems.
4. Study the different interfaces using Embedded Microcontroller.
5. Intend and analysis of real time operating system.

Expt. No.	Description of the experiments
1	System design using PIC Micro controller and its applications.
2	Testing of RTOS environment and system programming using ARM7 Processor.
3	System design using 8051 Micro Controller, 8086 Micro Processor.
4	RTC using PIC Micro Controller.
5	Elevator controller using PIC Micro Controller.
6	Modern Train Controller using PIC micro controller.
7	Study of MSP430 and 8086-16 bit Microprocessor its applications
8	Designing of Wireless Network using Embedded System.
9	Sensor design using simulation tools.
10	Study of 32 bit ARM7 microcontroller RTOS and its applications

Total Practical Hours 45

Course Outcome

CO1: Design various analog / digital transceiver systems and control different process.
CO2: Propose interfaces using embedded Microcontroller.
CO3: Experiment Wireless Network Using Embedded Systems.
CO4: Analyze the system using 8086 and 8051 Microcontroller.
CO5: Design and Analysis of Real Time Operating System

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SEMESTER-II

PROGRAMME	COURSE CODE	NAME OF THE COURSE	L	T	P	C
M.E	20AE2201	ANALOG INTEGRATED CIRCUIT DESIGN	3	0	0	3

Course Objectives

1. Design the single stage amplifiers using pmos and nmos driver circuits with different loads.
2. Analyze high frequency concepts of single stage amplifiers and noise characteristics associated with differential amplifiers.
3. Study the different types of current mirrors and to know the concepts of voltage and current reference circuits.
4. Gain the various applications in operational amplifier.
5. Learn the different concepts in stability and frequency compensation

Unit	Description	Instructional hours
I	**SINGLE STAGE AMPLIFIERS** Basic MOS physics and equivalent circuits and models, CS, CG and Source Follower differential with active load, Cascode and folded cascode configurations with active load, Design of differential and cascode amplifiers – to meet specified SR, noise, gain, BW, ICMR and power dissipation, voltage swing, High gain amplifier, structures.	9
II	**HIGH FREQUENCY AND NOISE OF CHARACTERISTICS AMPLIFIERS** Miller effect, association of poles with nodes, frequency response of CS, CG and source follower, cascode and differential pair stages, Statistical characteristics of noise, noise in single stage amplifiers, noise in differential amplifiers.	9
III	**FEEDBACK AND ONE STAGE OPERATIONAL AMPLIFIERS** Properties and types of negative feedback circuits, effect of loading in feedback networks, operational amplifier performance parameters, One-stage Op Amps, Two-stage Op Amps, Input range limitations, Gain boosting, slew rate, power supply rejection, noise in Op Amps.	9
IV	**STABILITY AND FREQUENCY COMPENSATION OF TWO STAGE AMPLIFIER** Analysis of two stage Op amp – two stage Op amp single stage CMOS Cs as second stage and using cascode second stage, multiple systems, Phase Margin, Frequency Compensation, and Compensation of two stage Op Amps, Slewing in two stage Op Amps, Other compensation techniques.	9
V	**BANDGAP REFERENCES** Current sinks and sources, Current mirrors, Wilson current source, Wildar current source, Cascode current source, Design of high swing cascode sink, current amplifiers, Supply independent biasing, temperature independent references, PTAT and CTAT current generation, Constant-Gm Biasing.	9
	Total instructional hours	**45**

Course Outcomes

CO1: Design and analysis of amplifiers.
CO2: Aquire of frequency response and noise analysis.
CO3: Familiarize the Operational Amplifiers.
CO4: Compose different types of Biasing Circuits.
CO5: Gain knowledge about the engineering applications of Analog Integrated Circuits

TEXT BOOKS:

T1. Behzad Razavi, "Design of Analog CMOS Integrated Circuits", Tata McGraw Hill, 2001
T2. Willey M.C. Sansen, "Analog Design Essentials", Springer, 2006.

REFERENCE BOOKS:

R1. Grebene, "Bipolar and MOS Analog Integrated Circuit Design", John Wiley & sons,Inc.,2003.
R2. Phillip E.Allen, Douglas R.Holberg, "CMOS Analog Circuit Design", Oxford University Press, 2nd Edition, 2002.
R3. Jacob Baker "CMOS: Circuit Design, Layout, and Simulation", Wiley IEEE Press, 3rd Edition, 2010..

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PROGRAMME	COURSE CODE	NAME OF THE COURSE	L	T	P	C
M.E	20AE2202	VLSI DESIGN TECHNIQUES	3	0	0	3

COURSE OBJECTIVE

To impart knowledge on

1. To understand the fundamentals of MOS transistor theory.
2. To analyze and design the CMOS technologies.
3. To study and discuss characteristics and performance estimation.
4. To study and understand the VLSI system components.
5. To understand Verilog programming.

Unit	Description	Instructional Hours
I	**INTRODUCTION TO MOS TRANSISTOR THEORY** MOS transistors, CMOS logic, MOS transistor theory–Introduction, Enhancement mode transistor action, Ideal I-V characteristics, Simple MOS capacitance Models, Detailed MOS gate capacitance model, Detailed MOS Diffusion capacitance model,Non ideal I-V effects, DC transfer characteristics, VLSI Design flow	9
II	**CMOS TECHNOLOGY AND DESIGN RULE** CMOS fabrication and Layout, CMOS technologies, P-Well process, N-Well process, twin-tub process, MOSlayers stick diagrams and Layout diagram, Layout design rules, Latch up in CMOS circuits, CMOS process enhancements, Technology–related CAD issues, Fabrication and packaging.	9
III	**CIRCUIT CHARACTERISATION & PERFORMANCE ESTIMATION** Determination of Pull-up to Pull-down ratio for NMOS inverter, super buffers, Driving large capacitance loads,Circuits families, transmission gates, Delay estimation, Power dissipation, Design margin, Scaling of MOSCircuits.	9
IV	**VLSI SYSTEM COMPONENTS CIRCUITS** Multiplexers, Decoders, comparators, priority encoders, Shift registers. Arithmetic circuits– Ripple carryadders, Carry look ahead adders, High-speed adders, Multiplier	9
V	**VERILOG HARDWARE DESCRIPTION LANGUAGE** Overview of digital design with Verilog HDL, hierarchical modeling concepts, basic concepts, modules and port definitions, gate level modeling, data flow modeling, behavioral modeling, task & functions, Test Bench.	9
	TOTAL INSTRUCTIONAL HOURS	**45**

COURSE OUTCOME

CO1: Identify various MOS transistor theory
CO2: Analyze the CMOS technology and to design.
CO3: Design and analyze circuit characteristics and Performance.
CO4: Design the VLSI system components and circuits.
CO5: Create models using Verilog programming.

TEXT BOOKS:

T1 Neil H.E.Weste, David Harris and Ayan Banerjee, "CMOS VLSI Design a circuits and systems perspective, Third Edition, Pearson Education, 2010

T2 Douglas A.Pucknell and Kamran Eshraghian, "Basic VLSI Design", Third Edition, Prentice-Hall of India 2004.

REFERENCES:

R1 Samir Palnitkar, "Verilog HDL a Guide to Digital Design and Synthesis", Second Edition, Pearson Education, 2010.

R2 John P.Uyemura "Introductionto VLSI Circuits and Systems", Wiley India Edition, 2006.

R3 Neil H.E. Weste and Kamran Eshraghian, Principles of CMOS VLSI Design, Pearson Education ASIA, 2nd edition, 2000.

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PROGRAMME	COURSE CODE	NAME OF THE COURSE	L	T	P	C
M.E	20AE2001	VLSI DESIGN LABORATORY	0	0	4	2

Course Objective

1. Learn new software tools for VLSI.
2. Study various design methods for VLSI circuits.
3. Gain the knowledge about circuit designing.
4. Analyze various applicationsusing VHDL and Verilog.
5. Analysis the digital system and simulator.

EXPT. No	Description of the Experiments
1.	Design and Simulation of Arithmetic /logic operator circuits using verilog/VHDL
2.	Design and 8-bit signed multiplication algorithm using verilog / VHDL
3.	Modeling of Combinational/Sequential Circuits Using Verilog HDL
4.	Simulation of Digital Circuits using Xilinx ISE.
5.	Design and Simulation of Digital Circuits using VHDL and Porting them into FPGA.
6.	Layout of Simple NMOS/CMOS Circuits.
7.	Analysis of Asynchronous and clocked synchronous sequential circuits.
8.	Design and Implementation of ALU in FPGA using VHDL and Verilog.
9.	Modeling of Sequential Digital system using Verilog and VHDL.
10.	Modeling of MAC unit using verilog / VHDL

Total Practical Hours 45

Course Outcome

CO1: Use the software tools for designing and simulation.
CO2: Design the various VLSI circuits using VHDL programming.
CO3: Familiarize the applications of VLSI circuits.
CO4: Analysis the MAC unit using verilog.
CO5: Design the VLSI circuits using Xillinx ISE tool.

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SEMESTER-III

PROGRAMME	COURSE CODE	NAME OF THE COURSE	L	T	P	C
M.E	20AE3901	DISSERTATION - I	0	0	20	10

Course Objective

1. Analyze a methodology to select a project and able to develop a hardware/software project.
2. Transform the ideas behind the project with clarity.
3. Validate the technical report.

Description of the project work

A candidate is permitted to work on projects in an Industrial / Research Organization, on the recommendations of the Head of the Department concerned.

A project must be selected either from research literature published list or the students themselves may propose suitable topics in consultation with their guide.

The aim of the project work is to strengthen the comprehension of principles by applying them to a new problem which may be the design and manufacture of a device, a research investigation or a design problem.

The project work shall be supervised by a supervisor of the department, (and an expert in industry if it is a industrial project), and the student shall be instructed to meet the supervisor periodically and to attend the review committee meeting for evaluation of the progress.

In case of candidates not completing Phase-I of project work successfully, the candidates can undertake Phase-I again in the subsequent semester. In such cases the candidates can enroll for Phase-II, only after successful completion of Phase-I.

The Project report shall be prepared and submitted according to the approved guidelines as given by the Controller of Examination and bonafied duly signed by Supervisor and the Head of the Department.

Course Outcome

CO1: Realize the skills acquired in the previous semesters to solve complex engineering problems.
CO2: Build up an innovative model / prototype of an idea related to the field of specialization.
CO3: Create the work individually to identify, troubleshoot and build products for environmental and societal issues.
CO4: Effective presentation of ideas with clarity.
CO5: Evaluate surveys towards developing a product which helps in life time learning.

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SEMESTER IV

PROGRAMME	COURSE CODE	NAME OF THE COURSE	L	T	P	C
M.E	20AE4901	DISSERTATION - II	0	0	30	15

Course Objective

1. Analyze a methodology to select a project and able to develop a hardware/software project.
2. Transform the ideas behind the project with clarity.
3. Validate the technical report.

Description of the project work

The Project work (Phase II) shall be pursued for a minimum prescribed period as per regulation.

The project work shall be supervised by a supervisor of the department, (and an expert in industry if it is a industrial project), and the student shall be instructed to meet the supervisor periodically and to attend the review committee meeting for evaluation of the progress.

The Project report shall be prepared and submitted according to the approved guidelines as given by the Controller of Examination and bonafied duly signed by Supervisor and the Head of the Department.

Course Outcome

CO1: Realize the skills acquired in the previous semesters to solve complex engineering problems.
CO2: Build up an innovative model / prototype of an idea related to the field of specialization.
CO3: Create the work individually to identify, troubleshoot and build products for environmental and societal issues.
CO4: Effective presentation of ideas with clarity.
CO5: Evaluate surveys towards developing a product which helps in life time learning.

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PROGRAMME	COURSE CODE	NAME OF THE COURSE	L	T	P	C
M.E.	20AE2304	PHYSICAL DESIGN OF VLSI CIRCUITS	3	0	0	3

Course Objective

1. To introduce the physical design concepts such as routing, placement, partitioning and packaging
2. To study the performance of circuits layout designs, compaction techniques

Unit	Description	Instructional hours
I	INTRODUCTION TO VLSI TECHNOLOGY Layout Rules-Circuit abstraction Cell generation using programmable logic array transistor chaining, Wein Berger arrays and gate matrices-layout of standard cells gate arrays and sea of gates, field programmable gate array(FPGA)-layout methodologies Packaging-Computational Complexity - Algorithmic Paradigms.	9
II	PLACEMENT USING TOP-DOWN APPROACH Partitioning: Approximation of Hyper Graphs with Graphs, Kernighan-Lin Heuristic Ratio cut partition with capacity and i/o constrants. Floor planning: Rectangular dual floor planning hierarchical approach- simulated annealing- Floor plan sizing Placement: Cost function- force directed method- placement by simulated annealing partitioning placement- module placement on a resistive network – regular placement linear placement.	9
III	ROUTING USING TOP DOWN APPROACH Fundamentals: Maze Running- line searching- Steiner trees Global Routing: Sequential Approaches - hierarchial approaches - multi commodity flow based techniques - Randomised Routing- One Step approach - Integer Linear Programming Detailed Routing: Channel Routing - Switch box routing. Routing in FPGA: Array based FPGA- Row based FPGAs	9
IV	PERFORMANCE ISSUES IN CIRCUIT LAYOUT Delay Models: Gate Delay Models- Models for interconnected Delay- Delay in RC trees. Timing – Driven Placement: Zero Stack Algorithm- Weight based placement- Linear Programming Approach Timing riving Routing: Delay Minimization- Click Skew Problem- Buffered Clock Trees. Minimization: constrained via Minimization unconstrained via Minimization- Other issues in minimization	9
V	SINGLE LAYER ROUTING, CELL GENERATION AND COMPACTION Planar subset problem(PSP)- Single Layer Global Routing- Single Layer detailed Routing- Wire length and bend minimization technique – Over The Cell (OTC) Routing Multiple chip modules(MCM)- programmable Logic Arrays- Transistor chaining- Wein Burger Arrays- Gate matrix layout- 1D compaction- 2D compaction.	9
	Total instructional hours	**45**

Course Outcome

After completion of the course the learner will be able to
CO1: Explain different types of routing
CO2: Discuss performance issues in circuit layout
CO3: Outline 1D compaction- 2D compaction.

REFERENCE BOOKS:

R1. Preas M. Lorenzatti, "Physical Design and Automation of VLSI systems", The Benjamin Cummins Publishers, 1998.

R2. Sarafzadeh, C.K. Wong, "An Introduction to VLSI Physical Design", McGraw Hill Int. Edition 1995

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Second Semester- (List of Professional Electives I, II, III)

PROGRAMME	COURSE CODE	NAME OF THE COURSE	L	T	P	C
ME	19AE2303	ASIC AND FPGA DESIGN	3	0	0	3

Course Objective

1. Describe the design flow of different types of ASIC and PLD
2. Gain knowledge about floor planning, placement and routing in ASIC
3. Implement the digital design using Verilog and VHDL
4. Infer the architecture of different types of FPGA
5. Describe the design issues of SOC

Unit	Description	Instructional Hours
I	**OVERVIEW OF ASIC AND PLD** Types of ASICs - Design Flow - CAD tools used in ASIC Design - Programming Technologies: Antifuse - Static RAM - EPROM and EEPROM Technology, Programmable Logic Devices: ROMs and EPROMs - PLA - PAL. Gate Arrays - CPLDs and FPGAs	9
II	**ASIC PHYSICAL DESIGN** System partition -Partitioning - Partitioning Methods - Interconnect Delay Models and Measurement of Delay - Floor Planning - Placement - Routing : Global Routing - Detailed Routing - Special Routing - Circuit Extraction - DRC	9
III	**LOGIC SYNTHESIS, SIMULATION AND TESTING** Design Systems - Logic Synthesis - Half Gate ASIC -Schematic Entry - Low Level Design Language - PLA Tools - EDIF- CFI Design Representation. Verilog and Logic Synthesis - VHDL and Logic Synthesis - Types of Simulation - Boundary Scan Test - Fault Simulation - Automatic Test Pattern Generation.	9
IV	**FPGA** Field Programmable Gate Arrays- Logic Blocks, Routing Architecture , FPGA Design : FPGA Physical Design Tools -Technology Mapping - Placement & Routing - Register Transfer (RT) / Logic Synthesis - Controller/Data Path Synthesis - Logic Minimization	9
V	**SOC DESIGN** Design Methodologies – Processes and Flows - Embedded Software Development for SOC - Techniques for SOC Testing – Configurable SOC – Hardware / Software CoDesign - Case studies: Digital Camera, Bluetooth Radio / Modem, SDRAM and USB.	9
	Total Instructional Hours	**45**

Course Outcome

CO1: Summarize the concepts of ASIC and PLD
CO2: Apply the different high performance algorithms in ASICs
CO3: Demonstrate the synthesis, simulation and testing of digital systems
CO4: Outline the different architectures of FPGA
CO5: Discuss the design issues of SOC

TEXT BOOKS:

T1 - David A.Hodges, Analysis and Design of Digital Integrated Circuits ,3rd Edition, Tata Mc Graw Hill , 2004.

T2 - M.J.S. Smith: Application Specific Integrated Circuits, Pearson, 2003.

REFERENCE BOOKS:

R1 - Parag.K.Lala, Digital System Design using Programmable Logic Devices, BSP, 2003.

R2 - Wayne Wolf, FPGA-Based System Design, Prentice Hall PTR, 2004.

R3 - Sudeep Pasricha and NikilDutt, On-Chip Communication Architectures System on Chip Interconnect, Elsevier,2008.

R4 - Farzad Nekoogar and Faranak Nekoogar, From ASICs to SOCs: A Practical Approach, Prentice Hall PTR, 2003.

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PROGRAMME	COURSE CODE	NAME OF THE COURSE	L	T	P	C
M.E	20AE2308	WIRELESS ADHOC AND SENSOR NETWORKS	3	0	0	3

Course Objectives

1. To understand the basics of Ad-hoc & Sensor Networks.
2. To learn various fundamental and emerging protocols of all layers
3. To study about the issues pertaining to major obstacles in establishment and efficient management of Ad-hoc and sensor networks.
4. To understand the nature and applications of Ad-hoc and sensor networks.
5. To understand various security practices and protocols of Ad-hoc and Sensor Networks.

Unit	Description	Instructional Hours
I	**MAC & TCP IN AD HOC NETWORKS** Fundamentals of WLANs – IEEE 802.11 Architecture - Self configuration and Auto configuration-Issues in Ad-Hoc Wireless Networks – MAC Protocols for Ad-Hoc Wireless Networks – Contention Based Protocols - TCP over Ad-Hoc networks-TCP protocol overview - TCP and MANETs – Solutions for TCP over Ad-Hoc Networks.	9
II	**ROUTING IN AD HOC NETWORKS** Routing in Ad-Hoc Networks- Introduction-Topology based versus Position based Approaches-Proactive, Reactive, Hybrid Routing Approach-Principles and issues – Location services - DREAM – Quorums based location service – Grid – Forwarding strategies – Greedy packet forwarding – Restricted directional flooding- Hierarchical Routing- Issues and Challenges in providing QoS.	9
III	**MAC, ROUTING & QOS IN WIRELESS SENSOR NETWORKS** Introduction – Architecture - Single node architecture – Sensor network design considerations – Energy Efficient Design principles for WSNs – Protocols for WSN – Physical Layer : Transceiver Design considerations – MAC Layer Protocols – IEEE 802.15.4 Zigbee – Link Layer and Error Control issues - Routing Protocols – Mobile Nodes and Mobile Robots - Data Centric & Contention Based Networking – Transport Protocols & QOS – Congestion Control issues – Application Layer support	9
IV	**SENSOR MANAGEMENT** Sensor Management - Topology Control Protocols and Sensing Mode Selection Protocols - Time synchronization - Localization and positioning – Operating systems and Sensor Network programming – Sensor Network Simulators.	9
V	**SECURITY IN AD HOC AND SENSOR NETWORKS** Security in Ad-Hoc and Sensor networks – Key Distribution and Management – Software based Anti-tamper techniques – water marking techniques – Defense against routing attacks - Secure Adhoc routing protocols – Broadcast authentication WSN protocols – TESLA – Biba – Sensor Network Security Protocols – SPINS	9
	Total Instructional Hours	**45**

Course Outcomes

CO1	Identify different issues in wireless ad hoc and sensor networks.
CO2	Analyze protocols developed for ad hoc and sensor networks.
CO3	Identify and address the security threats in ad hoc and sensor
CO4	Establish a Sensor network environment for different type of applications.
CO5	Understand the security in Ad hoc and Sensor networks

TEXT BOOKS:

T1 C.Siva Ram Murthy and B.S.Manoj, "Ad Hoc Wireless Networks – Architectures and Protocols", Pearson Education, 2004.

T2 Waltenegus Dargie, Christian Poellabauer, "Fundamentals of Wireless Sensor Networks Theory and Practice", John Wiley and Sons, 2010.

REFERENCE BOOKS:

R1 Carlos De Morais Cordeiro, Dharma Prakash Agrawal "Ad Hoc and Sensor Networks: Theory and Applications (2nd Edition), World Scientific Publishing, 2011.

R2 C.K.Toh, "Ad Hoc Mobile Wireless Networks", Pearson Education, 2002.

R3 Holger Karl, Andrea's willig, "Protocols and Architectures for Wireless Sensor Networks, John Wiley & Sons, Inc .2005.

R4 Subir Kumar Sarkar, T G Basavaraju, C Puttamadappa, "Ad Hoc Mobile Wireless Networks", Auerbach Publications, 2008.

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PROGRAMME	COURSE CODE	NAME OF THE COURSE	L	T	P	C
M.E	20AE2310	SATELLITE COMMUNICATIONS AND NAVIGATION SYSTEMS	3	0	0	3

COURSE OBJECTIVE

To impart knowledge on

1. Understand the necessity for satellite based communication, the essential elements involved and the transmission methodologies.
2. Understand the different interferences and attenuation mechanisms affecting the satellite link design.
3. Expose the advances in satellite based navigation, GPS and the different application scenarios..

Unit	Description	Instructional Hours
I	**ELEMENTS OF SATELLITE COMMUNICATION** Satellite Systems, Orbital description and Orbital mechanics of LEO, MEO and GSO, Placement of a Satellite in a GSO, Antennas and earth coverage, Altitude and eclipses, Satellite drift and station keeping, Satellite – description of different Communication subsystems, Bandwidth allocation.	9
II	**SATELLITE SPACE SEGMENT AND ACCESS** Introduction; attitude and orbit control system; telemetry, tracking and command; power systems, communication subsystems, antenna subsystem, equipment reliability and space qualification, Multiple Access: Demand assigned FDMA - spade system - TDMA - satellite switched TDMA –CDMA.	9
III	**SATELLITE LINK DESIGN** Basic link analysis, Interference analysis, Rain induced attenuation and interference, Ionospheric characteristics, Link Design: System noise temperature and G/T ratio, Downlink and uplink design, C/N, Link Design with and without frequency reuse, link margins, Error control for digital satellite link.	9
IV	**SATELLITE BASED BROADBAND COMMUNICATION** VSAT Network for Voice and Data – TDM/TDMA, SCPC/DAMA, Elements of VSAT Network, Mobile and Personal Communication Services, Satellite based Internet Systems, Multimedia Broadband Satellite Systems, UAVs.	9
V	**SATELLITE NAVIGATION AND GLOBAL POSITIONING SYSTEM** Radio and Satellite Navigation, GPS Position Location Principles of GPS Receivers and Codes, Satellite Signal Acquisition, GPS Receiver Operation and Differential GPS, INS, Indian Remote Sensing and ISRO GPS Systems.	9
	TOTAL INSTRUCTIONAL HOURS	**45**

COURSE OUTCOME

After completion of the course the learner will be able to

CO1: Demonstrate an understanding of the basic principles of satellite based communication the essential elements involved and the transmission methodologies.

CO2: Familiarize with satellite orbits, placement and control, satellite link design and the communication system components.

CO3: Demonstrate an understanding of the different interferences and attenuation mechanisms affecting the satellite link design.

CO4: Demonstrate an understanding of the different communication, sensing and navigational applications of satellite.

CO5: Familiarize with the implementation aspects of existing satellite based systems..

REFERENCES:

R1 Wilbur L. Pritchard, Hendri G. Suyderhoud and Robert A. Nelson, "Satellite Communication Systems Engineering", Prentice Hall/ Pearson, 2007.

R2 Timothy Pratt and Charles W.Bostain, "Satellite Communications", John Wiley and Sons, 2nd Edition, 2012.

R3 D.Roddy, "Satellite Communication", McGraw Hill, 4th Edition (Reprint), 2009

R4 Tri T Ha, "Digital Satellite Communication", McGraw Hill, 2nd Edition, 1990.

R5 B.N.Agarwal, "Design of Geosynchronous Spacecraft", Prentice Hall, 1993.

R6 Brian Ackroyd, "World Satellite Communication and Earth Station Design", BSP Professional Books, 1990.

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PROGRAMME	COURSE CODE	NAME OF THE COURSE	L	T	P	C
M.E.	20AE2313	Machine Learning	3	0	0	3

Course Objectives

1. To study the Mathematical background of machine learning
2. To enable the student to understand the concept of machine learning
3. To learn the fundamentals of different Neural network architectures
4. To know the machine learning application in wireless communication and bio-medical.
5. To expose the student to be familiar with a set of well-known supervised, semi-supervised and unsupervised learning algorithms.

Unit	Description	Instructional Hours
I	**MATHEMATICAL BACKGROUND** Linear Algebra – Arithmetic of matrices, Norms, Eigen decomposition, Singular value decomposition, Pseudo inverse, Component analysis. Probability theory – probability distribution, conditional probability, Chain rule, Bayes rule, Information theory, Structured Probabilistic models.	9
II	**MACHINE LEARNING BASICS** Supervised and Unsupervised learning, Capacity, Overfitting and Underfitting, Cross Validation, Linear regression, Logistic Regression, Regularization, Naive Bayes, Support Vector Machines (SVM), Decision tree, Random forest, K-Means Clustering, k nearest neighbor.	9
III	**NEURAL NETWORKS** Feedforward Networks , Back propagation, Convolutional Neural Networks-LeNet, AlexNet, ZF-Net, VGGNet, GoogLeNet, ResNet, Visualizing Convolutional Neural Networks, Guided Back propagation, Deep Dream, Deep Art, Fooling Convolutional Neural Networks. Recurrent Neural Network(RNN) – Back propagation through time (BPTT), Vanishing and Exploding Gradients.	9
IV	**ML IN WIRELESS AND SECURITY** Water-filling power allocation, Optimization for MIMO Systems, OFDM Systems and MIMO-OFDM systems. Optimization in beamformer design – Robust receive beamforming, Transmit downlink beamforming. Application: Radar for target detection, Array Processing, MUSIC, ML in Side channel analysis.	9
V	**ML IN BIO-MEDICAL** Machine Learning in Medical Imaging. Deep Learning for Health Informatics. Deep Learning Automated ECG Noise Detection and Classification System for Unsupervised Healthcare Monitoring. Techniques for Electronic Health Record (EHR) Analysis	9
	Total Instructional Hours	**45**

Course outcomes

- CO1 Demonstrate understanding of the mathematical principles underlying machine learning.
- CO2 Familiar with the different machine learning techniques and their use cases.
- CO3 In a position to formulate machine learning problems corresponding to different applications
- CO4 Able to recognize the characteristics of machine learning techniques that are useful to solve real-world problems.
- CO5 In a position to read current research papers, understand the issues and the machine learning based solution approaches.

REFERENCE BOOKS :

R1. Ian Goodfellow, Yoshua Bengio, and Aaron Courville, "Deep learning",Cambridge,MA, MIT Press, 2017.

R2. Tom M. Mitchell, "Machine Learning", McGraw Hill, 1997.

R3. Ethem Alpaydın, "Introduction to machine learning", MIT Press, 3rd Edition, 2014.

R4. M. N. Wernick, Y. Yang, J. G. Brankov, G. Yourganov and S. C. Strother, "Machine Learning in Medical Imaging", IEEE Signal Processing Magazine, vol. 27, no. 4, pp. 25-38, July 2010.

R5. Ravì et al., "Deep Learning for Health Informatics," IEEE Journal of Biomedical and Health Informatics, vol. 21, no. 1, pp. 4-21, Jan. 2017.

R6. R6-U. Satija, B. Ramkumar and M. S. Manikandan, "Automated ECG Noise Detection and Classification", IEEE Journal of Biomedical and Health Informatics PP(99), March 2017.

R6 -"System for Unsupervised Healthcare Monitoring," IEEE Journal of Biomedical and Health Informatics, vol. 22, no. 3, pp. 722-732, May 2018.

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PROGRAMME	COURSE CODE	NAME OF THE COURSE	L	T	P	C
M.E.	20AE2315	PCB DESIGN AND FABRICATION	3	0	0	3

Course Objectives

1. To expose the students to the basics of PCB design
2. To lead the new users of the software through a very simple design
3. To address the mechanical aspect of PCB design and to aid in understanding the design issues, manufacturing processes
4. To address the electrical aspect of PCB design
5. To expose the students to the state of art technology in PCB design and manufacturing.

Unit	Description	Instructional Hours
I	**BASICS OF PCB DESIGN AND TOOLS** Printed Circuit Board Fabrication- PCB cores and layer stack-up. PCB fabrication process- Photolithography and chemical etching, Mechanical Layer registration. Function of the Layout in the PCB Design Process. Design Files Created by Layout - Layout format files, Post process (Gerber) files, PCB assembly layers and files. Introduction to the Standards Organizations, Classes and Types of PCBs.	9
II	**PCB DESIGN FLOW USING CAD TOOL** Overview of Computer-Aided Design. Project structures and the layout toolset- Project Setup and Schematic Entry Details, the Layout Environment and Tool Set. Creating a Circuit Design with Capture-Starting a new project placing parts, Wiring (connecting) the parts, creating the Layout netlist in Capture. Designing the PCB with Layout- Starting Layout and importing the netlist, Performing a design rule check, Making a board outline, Placing the parts, Auto routing the board Manual routing, Cleanup Locking traces, Post processing the board design for manufacturing.	9
III	**DESIGN FOR MANUFACTURING** PCB Assembly and Soldering Processes- Component Placement and Orientation Guide, Component Spacing for Through-hole Devices. Component Spacing for Surface Mounted Devices SMDs, Mixed THD and SMD Spacing Requirements. Footprint and Padstack Design for PCB Manufacturability- Land Patterns for Surface-Mounted Devices- Land Patterns for Through-hole Devices, Padstack design, Hole-to-lead ratio, PTH land dimension (annular ring width), Clearance between plane layers and PTHs Soldermask and solder paste dimensions.	9
IV	**PCB DESIGN FOR SIGNAL INTEGRITY** Circuit Design Issues Not Related to PCB Layout, Issues Related to PCB Layout, Ground Planes and Ground Bounce, PCB Electrical Characteristics, PCB Routing Topics, Making and editing capture parts, The Capture Part Libraries, Types of Packaging, Pins, Part Editing Tools, Constructing Capture Parts, making and editing layout footprints.	9
V	**EMERGING ADDITIVE PROCESSES FOR PCB MANUFACTURING** Fundamentals of additive manufacturing, classification, advantages and standards on Additive manufacturing. Stereo lithography (SL), Stereo lithography (SL), Fused Deposition Modelling (FDM), Three Dimensional Printing (3DP), Materials, Applications. Voltera-V-one PCB double side Printer, Bot Factory- SV2-multi layer PCB printer, LPKF circuit board plotter and LDS Prototyping.	9
	Total Instructional Hours	**45**

Course Outcomes

- CO1 To understand the basics, industry standards organizations related to the design and fabrication of PCBs.
- CO2 Leads new users of the software through a very simple design
- CO3 To know and guide in designing plated through-holes, surface-mount lands, and Layout footprints in general.
- CO4 To know to construct Capture parts using the Capture Library Manager and Part Editor and the PSpice Model Editor.
- CO5 To understand and to fabricate PCBs

TEXT BOOKS:

T1 Kraig Mitzner, "Complete PCB Design Using OrCad Capture and Layout", Newness, 1st Edition, 2009.

T2 Simon Monk, "Make Your Own PCBs with EAGLE: From Schematic Designs to Finished Boards", McGraw-Hill Education TAB; 2nd Edition, 2017.

REFERENCE BOOKS:

R1 Douglas Brooks, "Signal Integrity Issues and Printed Circuit Board Design", Prentice Hall PTR, 2003.

R2 Lee W. Ritchey , John Zasio, Kella J. Knack, "Right the First Time: a Practical Handbook on High Speed PCB and System Design", Speeding Edge , 2003.

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PROGRAMME	COURSE CODE	NAME OF THE COURSE	L	T	P	C
M.E	20AE2316	TESTING OF VLSI CIRCUITS	3	0	0	3

Course Objective

1. Understand logic fault models.
2. Learn test generation for sequential and combinational logic circuits.
3. Study the concepts of design for testability.
4. Develop the self -test and their algorithms.
5. Acquire knowledge for the fault diagnosis.

Unit	Description	Instructional Hours
I	**TESTING AND FAULT MODELLING** Introduction to testing – Faults in Digital Circuits – Modelling of faults – Logical Fault Models –Fault detection – Fault Location – Fault dominance – Logic simulation – Types of simulation –Delay models – Gate Level Event – driven simulation.	9
II	**TEST GENERATION** Test generation for combinational logic circuits – Testable combinational logic circuit design – Test generation for sequential circuits – design of testable sequential circuits	9
III	**DESIGN FOR TESTABILITY** Design for Testability – Ad-hoc design – generic scan based design – classical scan based design– system level DFT approaches	9
IV	**SELF – TEST AND TEST ALGORITHMS** Built-In self-test – test pattern generation for BIST – Circular BIST – BIST Architectures – Testable Memory Design – Test Algorithms – Test generation for Embedded RAMs.	9
V	**FAULT DIAGNOSIS** Logical Level Diagnosis – Diagnosis by UUT reduction – Fault Diagnosis for Combinational Circuits– Self-checking design – System Level Diagnosis	9
	Total Instructional Hours	**45**

Course Outcome

CO1: Identify the testing and fault modeling.
CO2: Evaluate the test generation methods.
CO3: Prepare design for testability.
CO4: Apply the self-test algorithms.
CO5: Learn the fault diagnosis models.

TEXT BOOKS:

T1 A.L.Crouch, "Design Test for Digital IC"s and Embedded Core Systems", Prentice HallInternational, 2002.

T2 M.Abramovici, M.A.Breuer and A.D. Friedman, "Digital systems and Testable Design", JaicoPublishing House, 2002

REFERENCE BOOKS:

R1 M.L.Bushnell and V.D.Agrawal, "Essentials of Electronic Testing for Digital, Memory andMixed- Signal VLSI Circuits", Kluwer Academic Publishers, 2002

R2 P.K. Lala, "Digital Circuit Testing and Testability", Academic Press, 2002.

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PROGRAMME	COURSE CODE	NAME OF THE COURSE	L	T	P	C
M.E	20AE2317	LOW POWER VLSI DESIGN	3	0	0	3

Course Objective

1. Identify sources of power in an IC.
2. Understand the power reduction techniques based on technology independent and technology dependent.
3. Study the Power dissipation mechanism in various MOS logic style.
4. Design the suitable techniques to reduce the power dissipation.
5. Develop the memory circuits with low power dissipation.

Unit	Description	Instructional Hours
I	**POWER DISSIPATION IN CMOS** Physics of power dissipation in CMOS FET devices – Hierarchy of limits of power – Sources of power consumption – Static Power Dissipation, Active Power Dissipation - Designing for Low Power, Circuit Techniques For Leakage Power Reduction - Basic principle of low power design	9
II	**POWER OPTIMIZATION** Logic level power optimization – Circuit level low power design – Standard Adder Cells, CMOS Adders Architectures-BiCMOS adders - Low Voltage Low Power Design Techniques, Current Mode Adders -Types Of Multiplier Architectures, Braun, Booth and Wallace Tree Multipliers and their performance comparison	9
III	**DESIGN OF LOW POWER CMOS CIRCUITS** Computer arithmetic techniques for low power system – low voltage low power static Random access and dynamic Random access memories – low power clock, Inter connect and layout design – Advanced techniques – Special techniques	9
IV	**POWER ESTIMATION** Power Estimation techniques – logic power estimation – Simulation power analysis – Probabilistic power analysis.	9
V	**SYNTHESIS AND SOFTWARE DESIGN FOR LOW POWER** Synthesis for low power – Behavioral level transform – software design for low power	9
	Total Instructional Hours	**45**

Course Outcome

CO1: Learn the knowledge about power dissipation in CMOS circuits.
CO2: Under the concepts of power optimization techniques
CO3: Design the low power CMOS circuits
CO4: Evaluate the power estimation methods.
CO5: Learn the synthesis and software design for low power.

TEXT BOOKS:

T1 Gary Yeap, "Practical low power digital VLSI design", Kluwer, 1998.

T2 Kaushik Roy and S.C.Prasad, "Low power CMOS VLSI circuit design", Wiley, 2000 .

REFERENCE BOOKS:

R1 James B.Kulo, Shih-Chia Lin, "Low voltage SOI CMOS VLSI devices and Circuits", John Wiley and sons, inc. 2001.

R2 A.P.Chandrasekaran and R.W.Broadersen, "Low power digital CMOS design", Kluwer,1995

R3 DimitriosSoudris, C.Pignet, Costas Goutis,"Designing CMOS Circuits for Low Power"Kluwer, 2002.

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PROGRAMME	COURSE CODE	NAME OF THE COURSE	L	T	P	C
M.E	20AE2318	SYSTEM ON CHIP DESIGN	3	0	0	3

Course Objective

1. Understand the basic concepts of SoC design.
2. Learn the system level modeling methods.
3. Study the concepts of hardware software co design.
4. Acquire the knowledge about synthesis.
5. Learn the soc verification and testing methods.

Unit	Description	Instructional Hours
I	**INTRODUCTION** Introduction to SoC Design, system level design, methodologies and tools, system hardware: IO, communication, processing units, memories; operating systems: prediction of execution, real time scheduling, embedded OS, middle ware; Platform based SoC design, multiprocessor SoC and Network on Chip, Low power SoC Design	9
II	**SYSTEM LEVEL MODELLING** SystemC: overview, Data types, modules, notion of time, dynamic process, basic channels, structure communication, ports and interfaces, Design with examples	9
III	**HARDWARE SOFTWARE CO-DESIGN** Analysis, partitioning, high level optimisations, real-time scheduling, hardware acceleration, voltage scaling and power management; Virtual platform models, co-simulation and FPGAs for prototyping of HW/SW systems	9
IV	**SYNTHESIS** System synthesis: Transaction Level Modelling (TLM) based design, automatic TLM generation and mapping, platform synthesis; software synthesis: code generation, multi task synthesis, internal and external communication; Hardware synthesis: RTL architecture, Input models, estimation and optimization, resource sharing and pipelining and scheduling	9
V	**SOC VERIFICATION AND TESTING** SoC and IP integration, Verification : Verification technology options, verification methodology, overview: system level verification, physical verification, hardware/software co-verification; Test requirements and methodologies, SoC design for testability - System modeling, test power dissipation, test access mechanism	9
	Total Instructional Hours	**45**

Course Outcome

CO1: Acquire the knowledge of soc fundamentals.
CO2: Model and specify systems at high level of abstraction.
CO3: Understand hardware, software co design methods.
CO4: Appreciate the co-design approach and virtual platform models.
CO5: Learn the Soc verification and testing methods.

TEXT BOOKS:

T1 D. Black, J. Donovan, SystemC: From the Ground Up, Springer, 2004.

T2 D. Gajski, S. Abdi, A. Gerstlauer, G. Schirner, Embedded System Design: Modeling, Synthesis, Verification, Springer, 2009

REFERENCE BOOKS:

R1 Erik Larson, Introduction to advanced system-on-chip test design and optimization, Springer 2005

R2 Grotker, T., Liao, S., Martin, G. & Swan, S. System design with System C, Springer, 2002.

R3 Ghenassia, F. Transaction-level modeling with System C: TLM concepts and applications for embedded systems, Springer, 2010.

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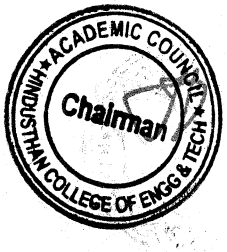

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PROGRAMME	COURSE CODE	NAME OF THE COURSE	L	T	P	C
M.E	20AE2319	COGNITIVE RADIO NETWORK	3	0	0	3

Course Objective

To understand the fundamentals of Software Defined radio and compare various SDR platforms.
To enable the student to understand the evolving paradigm of cognitive radio communication and the enabling technologies for its implementation.
To enable the student to understand the essential functionalities and requirements in designing software defined radios and their usage for cognitive communication
To analyze the various methods of implementing the Cognitive Radio functions
To exemplify the research challenges in designing a Cognitive Radio Network and the applications

Unit	Description	Instructional Hours
I	**SOFTWARE DEFINED RADIO AND ITS ARCHITECTURE** Definitions and potential benefits, software radio architecture evolution, technology tradeoffs and architecture implications. Essential functions of the software radio, basic SDR, hardware architecture, Computational processing resources, software architecture, top level component interfaces, interface topologies among plug and play modules.	9
II	**COGNITIVE RADIOS AND ITS ARCHITECTURE** Marking radio self-aware, cognitive techniques – position awareness, environment awareness in cognitive radios, optimization of radio resources, Artificial Intelligence Techniques, Cognitive Radio – functions, components and design rules, Cognition cycle – orient, plan, decide and act phases, Inference Hierarchy, Architecture maps, Building the Cognitive Radio Architecture on Software defined Radio Architechture.	9
III	**SPECTRUM SENSING AND IDENTIFICATION** Overview-Classification-Matched Filter , waveform based sensing - cyclo stationary based sensing - Energy detector based sensing - Radio Identifier - Cooperative Sensing -Spectrum Opportunity Detection , Fundamental Trade-offs: Performance versus Constraint , MAC Layer Performance Measures, Global Interference Model, Local Interference Model, Fundamental Trade-offs: Sensing Accuracy versus Sensing Overhead.	9
IV	**USER COOPERATIVE COMMUNICATIONS** User Cooperation and Cognitive Systems , Relay Channels: General Three-Node Relay Channel, Wireless Relay Channel , User Cooperation in Wireless Networks: Two-User Cooperative Network, Cooperative Wireless Network , Multihop Relay Channel	9
V	**INFORMATION THEORETICAL LIMITS ON CR NETWORKS** Types of Cognitive Behavior, Interference-Avoiding Behavior: Spectrum Interweave, Interference-Controlled Behavior: Spectrum Underlay, Underlay in Small Networks: Achievable Rates, Underlay in Large Networks: Scaling Laws, Interference-Mitigating Behavior: Spectrum Overlay, Opportunistic Interference Cancellation, Asymmetrically Cooperating Cognitive Radio Channels.	9
	Total Instructional Hours	**45**

Course Outcome

After completion of the course the learner will be able to

CO1: Appreciate the motivation and the necessity for cognitive radio communication strategies.
CO2: Demonstrate understanding of the enabling technologies for its implementation
CO3: Demonstrate understanding of the essential functionalities and requirements in designing software defined radios and their usage for cognitive communication.
CO4: Evolve new techniques and demonstrate their feasibility using mathematical validations and simulation tools.
CO5: Interpret the impact of the evolved solutions in future wireless network design.

REFERENCE BOOKS:

R1 Alexander M. Wyglinski, Maziar Nekovee, And Y. Thomas Hou, "Cognitive Radio Communications and Networks - Principles And Practice", Elsevier Inc. , 2010.
R2 Kwang-Cheng Chen and Ramjee Prasad, "Cognitive Radio Networks", John Wiley & Sons, Ltd, 2009.
R3 Khattab, Ahmed, Perkins, Dmitri, Bayoumi, Magdy, "Cognitive Radio Networks - From Theory to Practice", Springer Series, Analog Circuits and Signal Processing, 2009.
R4 J. Mitola, "Cognitive Radio: An Integrated Agent Architecture for software defined radio", Doctor of Technology thesis, Royal Inst. Technology, Sweden 2000.
R5 Simon Haykin, "Cognitive Radio: Brain –empowered wireless communications", IEEE Journal on selected areas in communications, Feb 2005.

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Third Semester (List of Professional Electives IV, V)

Programme	Course Code	Name of the Course	L	T	P	C
ME	20AE3301	INTELLIGENT SYSTEMS AND CONTROL	3	0	0	3

Course Objective

1. Introduce about Neural Networks.
2. Classify on various neural network.
3. To learn about Neuro controller
4. Gain knowledge about fuzzy system
5. Build application on fuzzy controller.

Unit	Description	Instructional Hours
I	**NEURAL NETWORKS – I** Linear Neural network, Multilayer Neural Network, Back Propagation Algorithm, Nonlinear system analysis part I, Nonlinear System Analysis part II , Radial basis function network, Adaptive learning rate, weight update rules, Recurrent Network back propagation through time, self-organizing map- Multidimensional network.	9
II	**NEURAL NETWORKS - II** Associative memory networks: Training algorithms for pattern association. Auto associative, Hetero associative, Hopfield and iterative auto associative memory networks. Unsupervised Learning networks: Fixed weight competitive nets, Kohenen self-organizing feature map	9
III	**NEURO CONTROLLER -III** Neural controller a review, Network Inversion and Control, Neural model for robot manipulator, Indirect adaptive controller of robot manipulator, Adaptive Neural for affine system SISO, MIMO, Visual motor co- ordination with KSOM. Direct adaptive controller of manipulator.	9
IV	**FUZZY SYSTEMS- I** Introduction to fuzzy logic, classical set, Fuzzy sets. Fuzzy relations Fuzzy arithmetic and fuzzy measures - Fuzzy rule base and approximate reasoning, Fuzzy logic controller.	9
V	**FUZZY CONTROL -II** Fuzzy controller a review, Mamdani type flc and parameter optimization, Fuzzy controller for PH reactor, Fuzzy lyapunav controller- computing with words, Controller design for a T-S fuzzy model, Linear Controller using T-S fuzzy model.	9
	Total Instructional Hours	**45**

Course Outcome

CO1: Infer the concepts of Neural Networks.
CO2: Summarize the various neural networks architectures and its training algorithms
CO3: Design the neural network/fuzzy logic control for real time applications.
CO3: Discover the concept of fuzzy logic set theory.
CO4: Implement the fuzzy mechanism for suitable control problems.

TEXT BOOKS:

T1 Laurene V. Fausett, "Fundamentals of Neural Networks:Architectures, algorithms and applications", Pearson Education, New Delhi, 2004.
T2 Timothy J Ross, "Fuzzy Logic with Engineering Applications", John Willey and Sons, 2005.

REFERENCE BOOKS:

R1 S.N.Sivanandam & S.N Deepa., "Principles of soft computing" ,2nd edition, Wiley India Pvt Ltd , 2013.
R2 George J.Klir, Bo.Yuan, "Fuzzy Sets and Fuzzy logic: Theory and Applications", PHI Learning Pvt Ltd, 2012
R3 Zimmerman H.J., "Fuzzy set theory and its Applications", Allied Publishers, 2001.
R4 -Jack M. Zurada, "Introduction to Artificial Neural Systems", PWS Publishing Co, 2002

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PROGRAMME	COURSE CODE	NAME OF THE COURSE	L	T	P	C
M.E.	20AE3302	ADVANCED MICROPROCESSORS & MICROCONTROLLERS	3	0	0	3

Course Objective

1. To expose the students to the fundamentals of microprocessor architecture.
2. To explore the high performance features in CISC architecture
3. To familiarize the high performance features in RISC architecture
4. To introduce the basic features in Motorola microcontrollers.
5. To enable the students to understand PIC Microcontroller

Unit	Description	Instructional Hours
I	**MICROPROCESSOR ARCHITECTURE** Instruction Set – Data formats –Addressing modes – Memory hierarchy –register file – Cache – Virtual memory and paging – Segmentation- pipelining –the instruction pipeline – pipeline hazards – instruction level parallelism – reduced instruction set –Computer principles – RISC versus CISC.	9
II	**HIGH PERFORMANCE CISC ARCHITECTURE – PENTIUM** CPU Architecture- Bus Operations – Pipelining – Brach predication – floating point unit- Operating Modes –Paging – Multitasking – Exception and Interrupts – Instruction set – addressing modes – Programming the Pentium processor.	9
III	**HIGH PERFORMANCE RISC ARCHITECTURE – ARM** Organization of CPU – Bus architecture –Memory management unit - ARM instruction set- Thumb Instruction set- addressing modes – Programming the ARM processor.	9
IV	**MSP430 16 - BIT MICROCONTROLLER** The MSP430 Architecture- CPU Registers - Instruction Set, On-Chip Peripherals - MSP430 - Development Tools, ADC - PWM - UART - Timer Interrupts - System design using MSP430Microcontroller.	9
V	**PIC MICROCONTROLLER** CPU Architecture – Instruction set – interrupts- Timers- I2C Interfacing –UART- A/D Converter –PWM and introduction to C-Compilers.	9
	Total Instructional Hours	**45 Hours**

Course Outcome

CO1: To understand the fundamentals of microprocessor architecture.
CO2: To know and appreciate the high performance features in CISC architecture.
CO3: To know and appreciate the high performance features in RISC architecture.
CO4: To perceive the basic features in Motorola microcontrollers.
CO5: To interpret and understand PIC Microcontroller.

TEXT BOOKS:

T1. Daniel Tabak , "Advanced Microprocessors", McGraw Hill.Inc., 1995.
T2. James L. Antonakos , "The Pentium Microprocessor" Pearson Education, 1997.

REFERENCE BOOKS:

R1. Steve Furber, "ARM System – On – Chip architecture", Addision Wesley, 2000.
R2. Andrew N.Sloss, Dominic Symes and Chris Wright "ARM System Developer's Guide : Designing and Optimizing System Software", First edition, Morgan Kaufmann Publishers, 2004.
R3 John. B. Peatman, "Design with PIC Microcontroller", Prentice hall, 1997.

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PROGRAMME	COURSE CODE	NAME OF THE COURSE	L	T	P	C
M.E.	20AE3305	High Speed Switching and Network	3	0	0	3

Course Objective

1. To understand the basics of switching technologies and their implementation LANs, ATM networks and IP networks
2. To understand the different queuing strategies and their impact on the blocking performances.
3. To understand the concepts of various packet switching architectures
4. To learn the fundamentals of Optical Switching Architectures
5. To exploit and integrate the best features of different architectures for high speed switching.

Unit	Description	Instructional Hours
I	**LAN SWITCHING TECHNOLOGY** Switching Concepts, LAN Switching, switch forwarding techniques - cut through and store and forward, Layer 3 switching, Loop Resolution, Switch Flow control, virtual LANs.	9
II	**QUEUES IN HIGH SPEED SWITCHES** Internal Queueing -Input, output and shared queueing, multiple queueing networks – combined Input, output and shared queueing - performance analysis of Queued switches	9
III	**PACKET SWITCHING ARCHITECTURES** Architectures of Internet Switches and Routers- Bufferless and buffered Crossbar switches, Multi-stage switching, Optical Packet switching; Switching fabric on a chip; Internally buffered Crossbars	9
IV	**. OPTICAL SWITCHING ARCHITECTURES** Need for Multilayered Architecture-, Layers and Sub-layers, Spectrum partitioning, Optical Network Nodes, Network Access Stations, Overlay Processor, Logical network overlays, Connection Management and Control	9
V	**IP SWITCHING** Addressing model, IP Switching types - flow driven and topology driven solutions, IP Over ATM address and next hop resolution, multicasting, Ipv6 over ATM.	9
	Total Instructional Hours	**45 Hours**

Course Outcome

After completion of the course the learner will be able to

CO1: Familiar with the basics of switching technologies and their implementation in LANs, ATM , IP and Optical networks.

CO2: Familiar with the different switching architectures and queuing strategies

CO3: Able to analyze switching networks based on their blocking performances and implementation complexities.

CO4: Able to identify suitable switch architectures for a specified networking scenario

CO5: To apply switching technologies, architectures and buffering strategies for designing high speed communication networks and analyse their performance

REFERENCE BOOKS :

R1 AchillePattavina, "Switching Theory: Architectures and performance in Broadband ATM networks ",John Wiley Sons Ltd, New York. 1998

R2 Thomas E. Stern, Georgios Ellinas, Krishna Bala, "Multiwavelength Optical Networks – Architecture, Design and control" , Cambridge University Press, 2nd Edition, 2009.

R3 Rich Siefert, Jim Edwards, "The All New Switch Book – The Complete Guide to LAN Switching Technology",Wiley Publishing, Inc., 2nd Edition, 2008

R4 Elhanany M. Hamdi, "High Performance Packet Switching architectures", Springer Publications, 2007.

R5 Christopher Y Metz, "Switching protocols & Architectures", McGraw - Hill Professional Publishing, New York, 1998.

R6 Rainer Handel, Manfred N Huber, Stefan Schroder, "ATM Networks - Concepts Protocols, Applications", Addison Wesley, New York, 3rd Edition, 1999

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PROGRAMME	COURSE CODE	NAME OF THE COURSE	L	T	P	C
M.E	20AE3306	PROGRAMMING LANGUAGES FOR EMBEDDED SOFTWARE	3	0	0	3

Course Objective

1. To understand the concepts and design to develop the low speed peripherals.
2. To understand the concepts of OOPS.
3. To Interpret the concepts of various CPP Programming methods
4. To learn the inheritance, overloading concepts.
5. To exploit PERL scripting..

Unit	Description	Instructional Hours
I	**EMBEDDED PERIPHERALS** Embedded 'C' Programming, Bitwise operations, Dynamic memory allocation, OS services, Linked stack and queue, Sparse matrices, Binary tree, Interrupt handling in C, Code optimization issues, Writing LED drivers, Drivers for serial port communication, Embedded Software Development Cycle and Methods (Waterfall, Agile).	9 hours
II	**OOPS PROGRAMMING TECHNIQUES** Object Oriented Programming: Introduction to procedural, modular, object-oriented and generic programming techniques, Limitations of procedural programming, objects, classes, data members, methods, data Encapsulation, data abstraction and information hiding, inheritance, polymorphism.	9 hours
III	**MEMORY ALLOCATION TECHNIQUES** CPP Programming: 'cin', 'cout', formatting and I/O manipulators, new and delete Operators, Defining a class, data members and methods, 'this' pointer, constructors, destructors, friend Function, dynamic memory allocation.	9 hours
IV	**OVERLOADING AND INHERITANCE** Need of operator overloading, overloading the assignment, Overloading using friends, type conversions, single inheritance, base and derived classes, friend classes, types of inheritance, hybrid inheritance, multiple inheritance, virtual base class, polymorphism, virtual functions.	9 hours
V	**TEMPLATES** Function template and class template, member function templates and template Arguments, Multiple Exceptions. Scripting Languages, PERL: Operators, Statements Pattern Matching.	9 hours

Course Outcomes

After completion of the course the learner will be able to

CO1: To develop drivers for low speed peripherals.
CO2: To describe OOPS concepts.
CO3: To develop CPP programming.
CO4: To Illustrate Inheritance, overloading concepts.
CO5: To explain PERL scripting

TEXT BOOKS

1. Michael J. Pont, Embedded C , Pearson Education, 2 nd Edition, 2008.
2. Michael Berman, Data structures via C++ , Oxford University Press, 2002.
3. Randal L. Schwartz, Learning Perl , O'Reilly Publications, 6 th Edition 2011.

REFERENCES

1. Robert Sedgewick, Algorithms in C++ , Addison Wesley Publishing Company, 1999. 20 M.Tech. in VLSI Design and Embedded Systems
2. Abraham Silberschatz, Peter B, Greg Gagne, Operating System Concepts , John Willey& Sons, 2005.
3. C.M. Krishna, Kang G. Shin, "Real Time Systems", McGraw - Hill International Editions, 1997
4. By Albert M. K. Cheng , "Real-time systems: scheduling, analysis, and verification" wiley

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PROGRAMME	COURSE CODE	NAME OF THE COURSE	L	T	P	C
M.E	20AE3309	ROBOTICS AND INTELLIGENT SYSTEMS	3	0	0	3

Course Objectives

1. To Teach the basic concepts in robotics.
2. To expose the various design aspects in robot grippers.
3. To make learn various drives and control systems.
4. To impart knowledge on machine vision systems.
5. To apply robot based concepts for automation

Unit	Description	Instructional Hours
I	**INTRODUCTION** Basic Concepts such as Definition, three laws, DOF, Misunderstood devices etc., Elements of Robotic Systems i.e. Robot anatomy, Classification, Associated parameters i.e. resolution, accuracy, repeatability, dexterity, compliance, RCC device, etc. Automation-Concept, Need, Automation in Production System, Principles and Strategies of Automation, Basic Elements of an Automated System, Advanced Automation Functions, Levels of Automations, introduction to automation productivity.	9
II	**ROBOT GRIPPERS** Types of Grippers, Design aspect for gripper, Force analysis for various basic gripper system. Sensors for Robots:- Characteristics of sensing devices, Selections of sensors, Classification and applications of sensors. Types of Sensors, Need for sensors and vision system in the working and control of a robot.	9
III	**DRIVES AND CONTROL SYSTEMS** Types of Drives, Actuators and its selection while designing a robot system. Types of transmission systems, Control Systems -Types of Controllers, Introduction to closed loop control .Control Technologies in Automation:- Industrial Control Systems, Process Industries Verses Discrete-Manufacturing Industries, Continuous Verses Discrete Control, Computer Process and its Forms. Control System Components such as Sensors, Actuators and others.	9
IV	**MACHINE VISION SYSTEM** Vision System Devices, Robot Programming: - Methods of robot programming, lead through programming, motion interpolation, branching capabilities, WAIT, SIGNAL and DELAY commands, subroutines, Programming Languages: Introduction to various types such as RAIL and VAL II etc, Features of type and development of languages for recent robot systems.	9
V	**MODELING AND SIMULATION FOR MANUFACTURING PLANT AUTOMATION** Introduction, need for system Modeling, Building Mathematical Model of a manufacturing Plant,Modern Tools- Artificial neural networks in manufacturing automation, AI in manufacturing,Fuzzy decision and control, robots and application of robots for automation.Artificial Intelligence:- Introduction to Artificial Intelligence, AI techniques, Need and application of AI. Other Topics in Robotics:- Socio-Economic aspect of robotisation. Economical aspects for robot design, Safety for robot and associated mass, New Trends & recent updates in robotics.	9
	Total Instructional Hours	**45**

Course Outcomes

CO1	Ability to implement simple concepts associated with Robotics and Automation
CO2	Ability to use various Robotic sub-systems
CO3	Ability to use kinematics and dynamics to design exact working pattern of robots
CO4	Ability to implement computer vison algorithms for robots
CO5	Be aware of the associated recent updates in Robotics

TEXT BOOKS:

T1 John J. Craig," Introduction to Robotics (Mechanics and Control)", Addison-Wesley, 2nd Edition, 2004

T2 Mikell P. Groover et. Al., "Industrial Robotics: Technology, Programming and Applications", McGraw – Hill International, 1986

REFERENCE BOOKS:

R1 Shimon Y. Nof, "Handbook of Industrial Robotics" , John Wiley Co,2001.

R2 Automation, "Production Systems and Computer Integrated Manufacturing", M.P. Groover, Pearson Education.

R3 Richard D. Klafter , Thomas A. Chemielewski, Michael Negin, "Robotic Engineering : An Integrated Approach" , Prentice Hall India, 2002.

R4 R.C. Dorf, "Handbook of design, manufacturing & Automation" John Wiley and Sons.

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PROGRAMME	COURSE CODE	NAME OF THE COURSE	L	T	P	C
M.E	20AE3311	5G Technology	3	0	0	3

Course Objectives

1 To introduce students with concepts, design issues in 5G networks
2 To study about architectures and protocols and the state-of-the–art developments in next generation wireless network technologies.
3 To Study various Multiple Access techniques for wireless channels.
4 To understand the relevance of MIMO techniques

Unit	Description	InstructionalHours
I	**5G CHANNEL MODEL** Modeling requirements and scenarios, Channel model requirements and Measurements, Propagation scenarios, METIS channel models, Map-based model, stochastic model, Comparison of Models	9
II	**MULTI-CARRIER WAVEFORMS FOR 5G** Filter-bank based multi-carrier (FBMC)- Principles, Transceiver block diagram, Frame structure, Resource structure, allocation, mapping. Universal filtered multi carrier (UFMC)- Principles, Transceiver structure, Frame and Resource structure, allocation, mapping. Generalized frequency division multicarrier (GFDM) – Principles, Transceiver Block diagram, Frame structure, Resource structure, allocation, mapping, MIMO-GFDM.	9
III	**MULTIPLE ACCESS TECHNIQUES IN 5G** Challenges in OFDM- NOMA – Principle- Superposition Coding, Successive Interference Cancellation, Power Domain NOMA, Sparse Code NOMA- types, Power Domain Sparse Code NOMA, Cooperative NOMA- Benefits and Challenges.	9
IV	**MASSIVE MIMO** Introduction-pilot design and channel estimation- uplink data transmission and downlink data transmission for Single cell systems and multi cell systems – capacity analysis.	9
V	**COOPERATIVE COMMUNICATION** Machine Type Communication (MTC), Device to Device Communication (D2D), 5G Narrowband IoT, Cloud Computing architecture and Protocols, Relaying: Cooperative NOMA- Benefits and Challenges, Half duplex relaying, Full duplex relaying, Amplify and forward relaying, Decode and forward relaying, Decode and forward relaying with PLNC, BER Analysis, Capacity Analysis.	9
	Total Instructional Hours	**45**

Course Outcomes

CO1 Able to analyze the performance of different channel models adopted in 5G wireless systems
CO2 Able to design a transceiver for Multicarrier waveforms
CO3 Able to analyze multiple access techniques in 5G networks
CO4 Able to design a pilot, estimate channels and analyze capacity for single cell and multicell Massive MIMO
CO5 Able to analyze different types of cooperative communications

REFERENCE BOOKS :

R1 AfifOsseiran, Jose.F.Monserrat and Patrick Marsch, "5G Mobile and Wireless Communications Technology", Cambridge University Press, 2016.

R2 Robert W. Heath Jr., Nuria González-Prelcic, SundeepRangan, WonilRoh,and Akbar M. Sayeed, "An Overview of Signal Processing Techniques for Millimeter Wave MIMO Systems", IEEE Journal of Selected Topics in Signal Processing, Vol. 10, No. 3, April 2016

R3 MinChulJu and Il-Min Kim, "Error Performance Analysis of BPSK Modulation in Physical- Layer Network-Coded Bidirectional Relay Networks", IEEE Transactions on Communications, Vol. 58, No. 10, October 2010.

R4 Shengli Zhang, Soung-Chang Liew, Patrick P.Lam, "Physical Layer Network Coding", Mobicom _06, Proceeding of the 12th International Conference on Mobile Computing and Networking, pp.358-365, Los Angeles, CA, USA, Sep.23-29,2006

R5 Thomas L. Marzetta, Erik G. Larsson, Hong Yang, HienQuoc Ngo, "Fundamentals of Massive MIMO", Cambridge University Press, 1 st Edition, 2016..

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PROGRAMME	COURSE CODE	NAME OF THE COURSE	L	T	P	C
M.E	20AE3312	IOT SYSTEM DESIGN AND SECURITY	3	0	0	3

Course Objectives

1. To understand the basics of IoT.
2. To get an idea about the various services provided by IoT.
3. To familiarize themselves with various communication techniques.
4. To get an idea of some application area where IoT can be applied.
5. To understand the various issues in IoT.

Unit	Description	Instructional Hours
I	**INTRODUCTION TO INTERNET OF THINGS** Rise of the machines – Evolution of IoT – Web 3.0 view of IoT – Definition and characteristics of IoT – Physical design of IoT – Logical design of IoT – IoT enabling technologies – IoT levels and deployment templates – A panaromic view of IoT applications.	9
II	**ARCHITECTURE OF IoT** Identifaction and Access to objects and services in the IoT environment(Current technologies for IoT naming-Solutions proposed by research projects-Research and Future development trends and forecast) – Middleware technologies for IoT system (IoT Ecosystem Overview – Horizontal Architecture Approach for IoT Systems-SOA-based IoT Middleware)Middleware architecture of RFID,WSN,SCADA,M2M–Challenges Introduced by 5G in IoT Middleware(Technological Requirements of 5G Systems-5G-based IoT Services and Applications Requirements-5G-based Challenges for IoT Middleware) - Perspectives and a Middleware Approach Toward 5G (COMPaaS Middleware) – Resource management in IoT	9
III	**SECURITY CONSIDERATIONS IN IOT SMART AMBIENT SYSTEMS** Security in Smart Grids and Smart Spaces for Smooth IoT Deployment in 5G (5G and the Internet of Things-Smart Spaces-Smart Grids Security and Privacy - Services that Need to Be Secure - Security Requirements -Security Attacks-Security Measures and Ongoing Research) - Security Challenges in 5G-Based IoT Middleware Systems(Security in 5G-Based IoT Middleware-Security Challenges Toward 5G).	9
IV	**IOT ENABLERS AND THEIR SECURITY AND PRIVACY ISSUES** Internet of Things layer wise Protocols and Standards- EPCglobal(architecture, specifications, industry adaptation, security and vulnerabilities , advantages and disadvantages)WirelessHART-Zigbee-Near Field Communication-6LoWPAN-Dash7-Comparative Analysis.	9
V	**APPLICATIONS AND CASE STUDIES** Home automations - Smart cities – Environment – Energy – Retail – Logistics – Agriculture – Industry - Health and life style – Case study	9
	Total Instructional Hours	**45**

Course Outcomes

CO1	Articulate the main concepts, key technologies, strength and limitations of IoT. CO2:
CO2	Identify the architecture, infrastructure models of IoT.
CO3	Analyze the core issues of IoT such as security, privacy and interoperability.
CO4	Analyze and design different models for network dynamics.
CO5	Identify and design the new models for market strategic interaction.

TEXT BOOKS:

T1 Honbo Zhou, "Internet of Things in the cloud:A middleware perspective", CRC press 2012.

T2 Vijay Madisetti and Arshdeep Bahga, "Internet of Things (A Hands-onApproach)", VPT, 1st Edition, 2014

REFERENCE BOOKS:

R1 Constandinos X. Mavromoustakis, George Mastorakis, Jordi Mongay Batalla, "Internet of Things (IoT) in 5G Mobile Technologies" Springer International Publishing, Switzerland, 2016.

R2 Dieter Uckelmann, Mark Harrison, Florian Michahelles, "Architecting the Internet of Things", Springer-Verlag Berlin Heidelberg, 2011.

R3 http://www.cse.wustl.edu/~jain/cse570-15/ftp/iot_prot/index.html

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PROGRAMME	COURSE CODE	NAME OF THE COURSE	L	T	P	C
M.E.	20AE3314	ELECTRONICS FOR SOLAR POWER	3	0	0	3

Course Objectives

1. Study the behavior of photovoltaic solar energy systems, focusing on the behavior of "stand-alone" systems.
2. Do a first order, conceptual design of a stand-alone system for a location anywhere in India
3. Introduce the hardware elements and their behavior.
4. Select battery for a PV system and battery sizing
5. Simulate standalone and grid tied PV system

Unit	Description	Instructional Hours
I	**INTRODUCTION TO SOLAR POWER** Semiconductor – properties - energy levels - basic equations of semiconductor devices physics - Basic characteristics of sunlight - Solar angles - day length - angle of incidence on tilted surface – Sun path diagrams – Equivalent circuit of PV cell, PV cell characteristics (VI curve, PV curve) - Maximum power point, Vmp, IMP, Voc, ISC – types of PV cell - Block diagram of solar photo voltaic system, PV array sizing.	9
II	**DC-DC CONVERTER** Principles of step-down and step-up converters – Analysis and design issues of buck, boost, buckboost and Cuk converters – time ratio and current limit control – Full bridge converter – Resonant and quasi – resonant converters.	9
III	**MAXIMUM POWER POINT TRACKING** Direct Energy transmission, Impedance Matching, Maximum Power Point Tracking (MPPT) - Function of MPPT, P&O method, INC Method, Fractional Open circuit voltage method, Fractional short circuit current method, parasitic capacitance and other MPPT techniques, Development of hardware, algorithms using processors for Standalone and Grid tied systems.	9
IV	**BATTERY** Types of Battery, Battery Capacity – Units of Battery Capacity-impact of charging and discharging rate on battery capacity-Columbic efficiency-Voltage Efficiency, Charging – Charge Efficiency, Charging methods, State of Charge, Charging Rates, Discharging - Depth of discharge-Discharge Methods, Circuits for Battery Management System (BMS), selection of Battery and sizing.	9
V	**SIMULATION OF PV MODULE & CONVERTERS** Simulation of PV module - VI Plot, PV Plot, finding VMP, IMP, Voc, Isc of PV module, Simulation of DC to DC converter -buck, boost, buck-boost and Cuk converters, standalone and grid tied photo voltaic system.	9
	Total Instructional Hours	**45**

Course Outcomes

- CO1 Ability to collect solar power characteristics at a given location
- CO2 Ability to design and realize dc-dc converters for solar power utilization
- CO3 Ability to design algorithms for improving solar power utilization
- CO4 Ability to deal with battery issues and selection
- CO5 Ability to design and simulate PV systems to validate its performance.

TEXT BOOKS:

T1 Chetan Singh Solanki, "Solar Photovoltaic: Fundamentals, Technologies and Applications", PHI Ltd., 2013.

T2 Tommarkvart, Luis castaner, "Solar cells; materials, manufacture and operation", Elsevier, 2005.

REFERENCE BOOKS:

R1 G.D .Rai, "Solar energy utilization ", Khanna publishes, 1993.

R2 Ned Mohan, Undeland and Robbin, "Power Electronics: converters, Application and Design", John Wiley and sons.Inc, Newyork, 1995.

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PROGRAMME	COURSE CODE	NAME OF THE COURSE	L	T	P	C
M.E	20AE3319	NANOELECTRONICS	3	0	0	3

Course Objective

1. To understand how transistor as Nano device
2. Learn the concepts of various forms of Nano Devices.
3. Study the concepts of Nano Sensors.
4. Acquire the knowledge Gas sensor materials.
5. Learn the concepts of Bio sensors.

Unit	Description	Instructional Hours
I	**SEMICONDUCTOR NANO DEVICES** Single-Electron Devices; Nano scale MOSFET – Resonant Tunneling Transistor - Single-Electron Transistors; Nanorobotics and Nanomanipulation; Mechanical Molecular Nanodevices; Nano computers: Optical Fibers for Nanodevices; Photochemical Molecular Devices; DNA-Based Nanodevices; Gas-Based Nanodevices	9
II	**ELECTRONIC AND PHOTONIC MOLECULAR MATERIALS** Preparation – Electroluminescent Organic materials - Laser Diodes - Quantum well lasers:- Quantum cascade lasers- Cascade surface-emitting photonic crystal laser- Quantum dot lasers - Quantum wire lasers:- White LEDs - LEDs based on nanowires - LEDs based on nanotubes - LEDs based on nanorods - High Efficiency Materials for OLEDs- High Efficiency Materials for OLEDs - Quantum well infrared photo detectors.	9
III	**THERMAL SENSORS** Thermal energy sensors -temperature sensors, heat sensors - Electromagnetic sensors - electrical resistance sensors, electrical current sensors, electrical voltage sensors, electrical power sensors, magnetism sensors - Mechanical sensors - pressure sensors, gas and liquid flow sensors, position sensors - Chemical sensors - Optical and radiation sensors	9
IV	**GAS SENSOR MATERIALS** Criteria for the choice of materials - Experimental aspects – materials, properties, measurement of gas sensing property, sensitivity; Discussion of sensors for various gases, Gas sensors based on semiconductor devices.	9
V	**BIOSENSORS** Principles - DNA based biosensors – Protein based biosensors – materials for biosensor applications - fabrication of biosensors - future potential	9
	Total Instructional Hours	**45**

Course Outcome

CO1: Acquire the knowledge of nano devices.
CO2: Understand the concepts of photonic molecular materials.
CO3: Learn the various types of thermal sensors.
CO4: Understand the concepts of gas sensor materials.
CO5: Understand the applications of different biosensors.

TEXT BOOKS:

T1 K.E. Drexler, "Nano systems", Wiley,1992.

REFERENCE BOOKS:

R1 M.C. Petty, "Introduction to Molecular Electronics", 1995.

R2 W. Ranier, "Nano Electronics and Information Technology", Wiley, 2003

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PROGRAMME	COURSE CODE	NAME OF THE COURSE	L	T	P	C
ME	20AE3320	MICRO-ELECTRO MECHANICAL SYSTEMS	3	0	0	3

Course Objective

1. To introduce students with concepts of MEMS products, sensors and fabrication.
2. To study about mechanics for MEMS design.
3. To Study about the electro static design and system issues for MEMS.
4. To understand the MEMS applications.
5. To understand the concepts of RF MEMS and optical MEMS.

Unit	Description	Instructional Hours
	UNIT I INTRODUCTION TO MEMS	
I	MEMS and Microsystems, Miniaturization, Typical products, Micro sensors, Micro actuation, MEMS with micro actuators, Micro-accelerometers and Micro fluidics, MEMS materials, Micro fabrication	9
	UNIT II MECHANICS FOR MEMS DESIGN	
II	Elasticity, Stress, strain and material properties, Bending of thin plates, Spring configurations, torsional deflection, Mechanical vibration, Resonance, Thermo mechanics – actuators, force and response time, Fracture and thin film mechanics	9
	UNIT III ELECTRO STATIC DESIGN AND SYSTEM ISSUES	
III	Electrostatics: basic theory, electro static instability. Surface tension, gap and finger pull up, Electro static actuators, Comb generators, gap closers, rotary motors, inch worms, Electromagnetic actuators. Bi-stable actuators. Electronic Interfaces, Feedback systems, Noise , Circuit and system issues	9
	UNIT IV MEMS APPLICATION	
IV	Case studies – Capacitive accelerometer, Peizo electric pressure sensor, Micro-fluidics application, Modeling of MEMS systems, CAD for MEMS.	9
	UNIT V INTRODUCTION TO OPTICAL AND RF MEMS	
V	Optical MEMS, - System design basics – Gaussian optics, matrix operations, resolution. Case studies, MEMS scanners and retinal scanning display, Digital Micro mirror devices. RF Memes – design basics, case study – Capacitive RF MEMS switch, performance issues	9
	Total Instructional Hours	**45**

Course Outcome

After completion of the course the learner will be able to

CO1: Able to demonstrate an understanding of the different aspects of micro-system design.
CO2: Familiar with Mechanical and the Electrostatic design aspects
CO3: Familiar with the different applications and their design basics
CO4: In a position to identify a suitable MEMS structure, material and fabrication procedure based on the application and functionality.
CO5: Capable of applying his knowledge and design tools and will be well practiced in design skills.

TEXT BOOKS:

R1 - Stephen Santeria, "Microsystems Design", Kluwer publishers, 2000.
R2 - N.P.Mahalik, "MEMS",Tata McGraw hill, 2007

REFERENCE BOOKS

R3 - Nadim Maluf, "An introduction to Micro electro mechanical system design", Artech House, 2000
R4 - Mohamed Gad-el-Hak, "The MEMS Handbook", CRC press Baco Raton,2000.
R5 - Tai Ran Hsu, "MEMS & Micro systems Design and Manufacture", Tata McGraw Hill, New Delhi, 2002.

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PROGRAMME	COURSE CODE	NAME OF THE COURSE	L	T	P	C
M.E.	20AE3401	ROBOTICS	3	0	0	3

Course Objectives

1. Understand robot locomotion and mobile robot kinematics.
2. Articulate perception in robotics
3. Outline mobile robot localization.
4. Understand mobile robot mapping.
5. Explain robot planning and navigation.

Unit	Description	Instructional Hours
I	**LOCOMOTION AND KINEMATICS** Introduction to Robotics – key issues in robot locomotion – legged robots – wheeled mobile robots – aerial mobile robots – introduction to kinematics – kinematics models and constraints – robot maneuverability	9
II	**ROBOT PERCEPTION** Sensors for mobile robots – vision for robotics – cameras – image formation – structure from stereo – structure from motion – optical flow – color tracking – place recognition – range data sensors, linear variable differential transformers (LVDT), Hall Effect sensors.	9
III	**MOBILE ROBOT LOCALIZATION** Introduction to localization – challenges in localization – localization and navigation – belief representation – map representation – probabilistic map-based localization – Markov localization – EKF localization – UKF localization – Grid localization – Monte Carlo localization – localization in dynamic environments	9
IV	**MOBILE ROBOT MAPPING** Autonomous map building – occupancy grip mapping – MAP occupancy mapping – SLAM – extended Kalman Filter SLAM – graph-based SLAM – particle filter SLAM – sparse extended information filter – fast SLAM algorithm.	9
V	**PLANNING AND NAVIGATION** Introduction to planning and navigation – planning and reacting – path planning – obstacle avoidance techniques – navigation architectures – basic exploration algorithms	9
	Total Instructional Hours	45

Course Outcomes

CO1: Understand robot locomotion and mobile robot kinematics.
CO2: Understand perception in robotics.
CO3: Apply robot localization techniques.
CO4: Apply robot mapping techniques.
CO5: Explain planning and navigation in robotics.

TEXT BOOKS:

T1. Gregory Dudekand Michael Jenkin, "Computational Principles of Mobile Robotics", Second Edition, Cambridge University Press, 2010.
T2. Howie Choset et al., "Principles of Robot Motion: Theory, Algorithms, and Implementations", A Bradford Book, 2005.

REFERENCE BOOKS:

R1. Maja J. Mataric, "The Robotics Primer", MIT Press, 2007.
R2. Roland Seigwart, "Introduction to autonomous mobile robots", Second Edition, MIT Press, 2011.
R3. Sebastian Thrun, Wolfram Burgard, and Dieter Fox, "Probabilistic Robotics", MIT Press, 2005.
R4. Mikell.P.Groover, "Industrial Robotics – Technology, Programming and applications", Tata McGraw Hill 2008.

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PROGRAMME	COURSE CODE	NAME OF THE COURSE	L	T	P	C
M.E.	20AE3402	ARTIFICIAL INTELLIGENCE AND OPTIMIZATION TECHNIQUES	3	0	0	3

Course Objectives

1. To introduce the techniques of computational methods inspired by nature, such as neural networks, genetic algorithms and other evolutionary computation systems, ant swarm optimization and artificial immune systems.
2. To present main rules underlying in these techniques.
3. To present selected case studies.
4. To adopt these techniques in solving problems in the real world.

Unit	Description	Instructional Hours
I	**NEURAL NETWORKS** Neural Networks: Back Propagation Network, generalized delta rule, Radial Basis Function Network, interpolation and approximation RBFNS, comparison between RBFN and BPN, Support Vector Machines: Optimal hyperplane for linearly separable patterns, optimal hyperplane for nonlinearly separable patterns, Inverse Modeling.	9
II	**FUZZY LOGIC SYSTEMS** Fuzzy Logic System: Basic of fuzzy logic theory , crisp and fuzzy sets, Basic set operation like union , interaction , complement , T-norm , T-conorm , composition of fuzzy relations, fuzzy if-then rules , fuzzy reasoning, Neuro-Fuzzy Modeling: Adaptive Neuro-Fuzzy Inference System (ANFIS) , ANFIS architecture , Hybrid Learning Algorithm.	9
III	**EVOLUTIONARY COMPUTATION & GENETIC ALGORITHMS** Evolutionary Computation (EC) – Features of EC – Classification of EC – Advantages – Applications. Genetic Algorithms: Introduction – Biological Background – Operators in GA-GA Algorithm – Classification of GA – Applications	9
IV	**ANT COLONY OPTIMIZATION** Ant Colony Optimization: Introduction – From real to artificial ants- Theoretical considerations – Convergence proofs – ACO Algorithm – ACO and model based search – Application principles of ACO.	9
V	**PARTICLE SWARM OPTIMIZATION** Particle Swarm Optimization: Introduction – Principles of bird flocking and fish schooling – Evolution of PSO – Operating principles – PSO Algorithm – Neighborhood Topologies – Convergence criteria – Applications of PSO, Honey Bee Social Foraging Algorithms, Bacterial Foraging Optimization Algorithm.	9
	Total Instructional Hours	45

Course Outcomes

CO1: Ability to design and train neural networks with different rules
CO2: Ability to devise fuzzy logic rules
CO3: Ability to implement genetic algorithms
CO4: Ability to implement ANT colony optimization technique for various problems
CO5: Ability to use PSO technique

TEXT BOOKS:

T1 David E. Goldberg, "Genetic Algorithms in search, Optimization & Machine Learning", Pearson Education, 2006
T2 Christopher M. Bishop, "Neural Networks for Pattern Recognition", Oxford University Press, 1995

REFERENCE BOOKS:

R1 N P Padhy, "Artificial Intelligence and Intelligent Systems", Oxford University Press, 2005.
R2 Engelbrecht, A.P., "Fundamentals of Computational Swarm Intelligence", Wiley, 2005.
R3 Kenneth A DeJong,"Evolutionary Computation A Unified Approach", Prentice Hall of India, New Delhi, 2006.
R4 Marco Dorigo and Thomas Stutzle, "Ant Colony optimization", Prentice Hall of India, New Delhi, 2004.

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